TEF6730A

Front-end for digital-IF car radio

Rev. 01 — 21 February 2007 Product data sheet

1. General description

The TEF6730A is a car radio tuner front-end for digital-IF reception, especially designed for co-operation with digital-IF DSP back-ends of the SAF773x and SAF778x families.

The FM tuner features single conversion to IF = 10.7 MHz and integrated image rejection; capable for FM 65 MHz to 108 MHz and weather band reception. The AM tuner features single conversion to IF = 10.7 MHz with an integrated AM front-end, capable for LW, MW and full SW reception. A combined AM/FM IF AGC amplifier provides a suitable IF signal to the ADC in IF DSP.

The device can be controlled via the fast-mode I^2C-bus (400 kHz) and includes autonomous tuning functions for easy control. No manual alignments are required.

2. Features

- FM mixer for conversion of FM RF to IF 10.7 MHz with large dynamic range, high image rejection and selectable mixer gain
- Selectable high or low injection of LO
- AGC PIN diode drive circuit for FM RF AGC with detection at RF and IF, including keyed AGC function
- RF input for weather band applications
- Integrated AM front-end LNA
- Integrated AM RF AGC for low desensitization and AGC PIN diode drive circuit with detection at RF and IF
- AM mixer for conversion of AM RF to IF 10.7 MHz
- AM/FM IF AGC amplifier with large dynamic range, gain controlled from IF DSP
- AM and FM front-end AGC information is available via the I^2C-bus
- Low phase noise local oscillator with reliable start-up behavior
- In-lock detection for optimized adaptive PLL tuning speed
- Programmable divider and mixer dividers for reception of FM (65 MHz to 108 MHz), weather band, AM LW, MW and full SW
- Two antenna DAAs
- Sequential state machine supporting all tuning actions including AFU for RDS
- Interfacing signals for IF AGC, FM keyed AGC, AFU and reference frequency to IF DSP for optimum system performance
- Software controlled flag outputs
- Selection of four I^2C-bus addresses
- Qualified in accordance with AEC-Q100

3. Quick reference data

Table 1. Quick reference data

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage							
V_{CCA}	analog supply voltage	on pins V_{CC}, $V_{CC(PLL)}$, $V_{CC(VCO)}$, $V_{CC(RF)}$, $V_{CC(IF)}$, FMMIXOUT1, FMMIXOUT2, AMMIXOUT1 and AMMIXOUT2		8	8.5	9	V
Current in FM mode							
$I_{CC(tot)}$	total supply current			-	85.3	-	mA
Current in AM mode							
$I_{CC(tot)}$	total supply current			-	114.7	-	mA
Antenna Digital Auto Alignment (DAA)							
DAA1: pin DAAOUT1[1]							
$G_{conv(DAA)}$	DAA conversion gain			0.1	-	2	
DAA2: pin DAAOUT2[2]							
$G_{conv(DAA)}$	DAA conversion gain			0.7	-	1.35	
Reference frequency							
External reference frequency, circuit inputs: pins FREF1 and FREF2							
f_{ext}	external frequency			-	100	-	kHz
Tuning system; see Table 28, Table 29, Table 30 and Table 31							
Voltage controlled oscillator							
$f_{VCO(min)}$	minimum VCO frequency		[3]	-	-	130	MHz
		application according to Figure 25	[3]	-	-	159.9	MHz
$f_{VCO(max)}$	maximum VCO frequency		[3]	256	-	-	MHz
C/N	carrier-to-noise ratio	f_{VCO} = 200 MHz; Δf = 10 kHz; Q = 30		94	98	-	dBc/√Hz
Timings							
t_{tune}	tuning time	Europe FM and US FM band; f_{ref} = 100 kHz; f_{RF} = 87.5 MHz to 108 MHz		-	0.75	1	ms
		AM MW band; f_{ref} = 20 kHz; f_{RF} = 0.53 MHz to 1.7 MHz		-	-	10	ms
$t_{upd(AF)}$	AF update time	cycle time for inaudible AF update including 1 ms mute start and 1 ms mute release time		-	6	6.5	ms
AM overall system parameters[4]							
$f_{i(RF)}$	RF input frequency	LW		144	-	288	kHz
		MW		522	-	1710	kHz
		SW		2.3	-	26.1	MHz
f_{IF}	IF frequency			-	10.7	-	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB		-	50	-	µV

Table 1. Quick reference data *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(RF)}$	RF input voltage	start level of wideband AGC				
		data byte AGC bits WBAGC[1:0] = 00	-	125	-	mV
		data byte AGC bits WBAGC[1:0] = 01	-	100	-	mV
		data byte AGC bits WBAGC[1:0] = 10	-	75	-	mV
		data byte AGC bits WBAGC[1:0] = 11	-	35	-	mV
$V_{i(RF)M}$	peak RF input voltage	start level of narrow-band AGC; m = 0				
		data byte AGC bits NBAGC[1:0] = 00	-	200	-	mV
		data byte AGC bits NBAGC[1:0] = 01	-	170	-	mV
		data byte AGC bits NBAGC[1:0] = 10	-	140	-	mV
		data byte AGC bits NBAGC[1:0] = 11	-	115	-	mV
IP2	second-order intercept point	referenced to receiver input	-	152	-	dBµV
IP3	third-order intercept point	referenced to receiver input				
		Δf = 40 kHz	-	130	-	dBµV
		Δf = 100 kHz	-	133	-	dBµV
α_{ripple}	ripple rejection	$V_{CC(ripple)}$ / V_{audio}; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 10 mV (RMS); $V_{i(RF)}$ = 1 mV to 1 V	-	40	-	dB
FM overall system parameters[5]						
$f_{i(RF)}$	RF input frequency	FM standard	65	-	108	MHz
		weather band	162.4	-	162.55	MHz
f_{IF}	IF frequency		-	10.7	-	MHz
V_{sens}	sensitivity voltage	B_{IF} = 170 kHz	-	2	-	µV
		threshold extension enabled; weak signal handling enabled (SAF7730 N231)	-	1.1	-	µV
$V_{i(RF)}$	RF input voltage	start level of wideband AGC				
		data byte AGC bits WBAGC[1:0] = 00	-	19	-	mV
		data byte AGC bits WBAGC[1:0] = 01	-	14	-	mV
		data byte AGC bits WBAGC[1:0] = 10	-	10	-	mV
		data byte AGC bits WBAGC[1:0] = 11	-	7	-	mV
$V_{i(RF)M}$	peak RF input voltage	start level of narrow-band AGC; m = 0				
		data byte AGC bits NBAGC[1:0] = 00	-	17	-	mV
		data byte AGC bits NBAGC[1:0] = 01	-	14	-	mV
		data byte AGC bits NBAGC[1:0] = 10	-	11	-	mV
		data byte AGC bits NBAGC[1:0] = 11	-	9	-	mV
IP3	third-order intercept point	Δf = 400 kHz	-	123	-	dBµV
α_{ripple}	ripple rejection	$V_{CC(ripple)}$ / V_{audio}; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 10 mV (RMS); $V_{i(RF)}$ = 500 µV	-	64	-	dB
			-	-	-	

[1] Conversion gain formula of DAA1: $V_{DAAOUT1} = \left(1.915 \times \frac{n}{128} + 0.1\right) \times V_{tune}$ where n = 0 to 127.

[2] Conversion gain formula of DAA2: $V_{DAAOUT2} = \left(0.693 \times \frac{n}{16} + 0.7\right) \times V_{DAAOUT1}$ where n = 0 to 15.

[3] The VCO frequency is determined by the external circuit at pins OSCFDB and OSCTNK.

[4] Based on 15 pF/60 pF dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, 2.5 kHz audio bandwidth, $f_{i(RF)}$ = 990 kHz, m = 0.3 and nominal maximum IF AGC gain, unless otherwise specified.

[5] Based on 75 Ω dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, de-emphasis = 50 µs, $f_{i(RF)}$ = 97.1 MHz, Δf = 22.5 kHz, nominal mixer gain and nominal maximum IF AGC gain, unless otherwise specified.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEF6730AHW	HTQFP64	plastic thermal enhanced thin quad flat package; 64 leads; body 10 x 10 x 1 mm; exposed die pad	SOT855-1

5. Block diagram

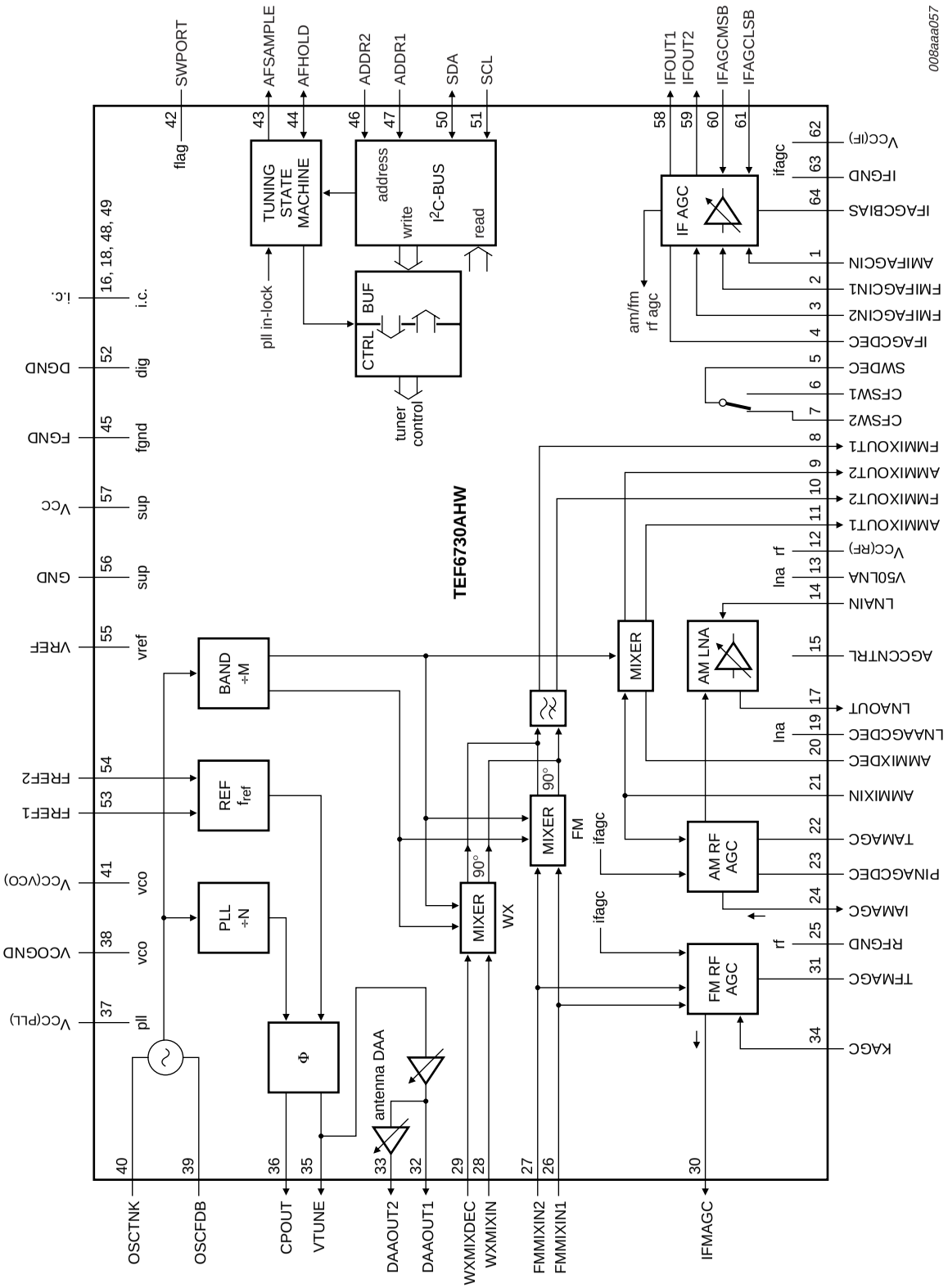


Fig 1. Block diagram of TEF6730AHW

6. Pinning information

6.1 Pinning

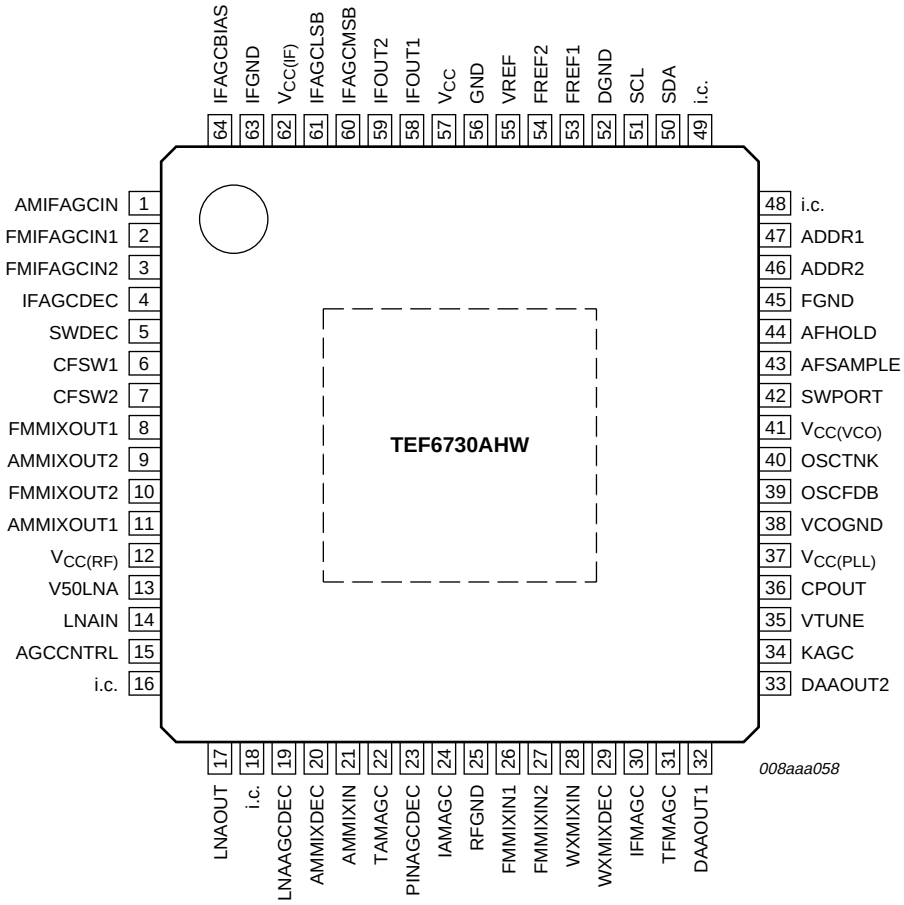


Fig 2. Pin configuration for HTQFP64

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
AMIFAGCIN	1	IF AGC amplifier AM input (10.7 MHz)
FMIFAGCIN1	2	IF AGC amplifier FM input 1 (10.7 MHz)
FMIFAGCIN2	3	IF AGC amplifier FM input 2 (10.7 MHz)
IFAGCDEC	4	IF AGC amplifier AM and FM decoupling
SWDEC	5	ceramic filter switch decoupling
CFSW1	6	ceramic filter switch 1
CFSW2	7	ceramic filter switch 2
FMMIXOUT1	8	FM mixer IF output 1 (10.7 MHz)
AMMIXOUT2	9	AM mixer IF output 2 (10.7 MHz)

Table 3. Pin description *…continued*

Symbol	Pin	Description
FMMIXOUT2	10	FM mixer IF output 2 (10.7 MHz)
AMMIXOUT1	11	AM mixer IF output 1 (10.7 MHz)
$V_{CC(RF)}$	12	AM/FM RF supply voltage
V50LNA	13	AM LNA supply voltage decoupling
LNAIN	14	AM LNA input
AGCCNTRL	15	AM LNA AGC pin
i.c.	16	internally connected; leave open
LNAOUT	17	AM LNA output
i.c.	18	internally connected; leave open
LNAAGCDEC	19	AM LNA AGC decoupling
AMMIXDEC	20	AM mixer decoupling
AMMIXIN	21	AM mixer input
TAMAGC	22	AM RF AGC time constant
PINAGCDEC	23	AM PIN diode AGC decoupling
IAMAGC	24	AGC current for AM PIN diode
RFGND	25	RF ground
FMMIXIN1	26	FM mixer input 1
FMMIXIN2	27	FM mixer input 2
WXMIXIN	28	weather band mixer input
WXMIXDEC	29	weather band mixer decoupling
IFMAGC	30	AGC current for FM PIN diode
TFMAGC	31	FM RF AGC time constant
DAAOUT1	32	antenna DAA output 1
DAAOUT2	33	antenna DAA output 2
KAGC	34	level input for FM keyed AGC function
VTUNE	35	tuning voltage input antenna DAA
CPOUT	36	charge pump output
$V_{CC(PLL)}$	37	tuning PLL supply voltage
VCOGND	38	VCO ground
OSCFDB	39	VCO feedback
OSCTNK	40	VCO tank circuit
$V_{CC(VCO)}$	41	VCO supply voltage
SWPORT	42	software controllable port output
AFSAMPLE	43	AF sample flag output
AFHOLD	44	AF hold flag output and input
FGND	45	reference frequency ground
ADDR2	46	address select input 2
ADDR1	47	address select input 1
i.c.	48	internally connected; leave open
i.c.	49	internally connected; leave open
SDA	50	I^2C-bus data line input and output

Table 3. Pin description *…continued*

Symbol	Pin	Description
SCL	51	I^2C-bus clock line input
DGND	52	digital ground
FREF1	53	reference frequency input 1
FREF2	54	reference frequency input 2
VREF	55	reference voltage noise decoupling
GND	56	ground
V_{CC}	57	supply voltage (8.5 V)
IFOUT1	58	IF AGC amplifier output 1
IFOUT2	59	IF AGC amplifier output 2
IFAGCMSB	60	MSB input for IF AGC amplifier gain setting
IFAGCLSB	61	LSB input for IF AGC amplifier gain setting
$V_{CC(IF)}$	62	IF AGC amplifier supply voltage
IFGND	63	IF AGC amplifier ground
IFAGCBIAS	64	bias voltage decoupling for IF AGC amplifier

7. Functional description

7.1 FM mixer 1

The FM quadrature mixer converts FM RF (65 MHz to 108 MHz) to an IF frequency of 10.7 MHz. The FM mixer provides high image rejection, a large dynamic range and selectable mixer gain. The image rejection can be selected between low injection of LO and high injection of LO via the I^2C-bus independently of the band selection. A separate RF input for weather band is available.

7.2 FM RF AGC

AGC detection is at the FM front-end mixer input and the AM/FM IF AGC amplifier input, both with programmable AGC thresholds. When the threshold is exceeded, the PIN diode drive circuit sources a current to an external PIN diode circuit, keeping the RF signal level constant.

Keyed AGC function is selectable via the I^2C-bus and uses the in-band level information from the IF DSP.

The AGC PIN diode drive circuit can optionally deliver a fixed current as a local function. In AM mode, the AGC PIN diode drive circuit can be set to generate a fixed source current into the external FM PIN diode circuitry.

7.3 Antenna DAA1 and DAA2

The antenna DAA1 measures the VCO tuning voltage and multiplies it with a factor defined by the 7-bit DAA1 setting to generate a tuning voltage for the FM antenna tank circuit. If a second FM tank circuit is applied, the tuning voltage can be derived from the antenna DAA2 output. The antenna DAA2 measures the output voltage of the antenna DAA1 and multiplies it with a factor defined by the 4-bit DAA2 setting.

7.4 AM LNA

The AM low noise amplifier is fully integrated.

7.5 AM RF AGC

The AM RF AGC is partially integrated. Detection is at the output of the AM LNA and at the input of the AM/FM IF AGC amplifier, both with programmable thresholds. First the integrated AGC reduces the gain of the LNA. After the LNA AGC, the PIN diode AGC takes over by sinking a current via an external PIN diode.

In FM mode, the AM AGC can be set to a fixed attenuation.

7.6 AM mixer

The large dynamic range AM mixer converts AM RF (144 kHz to 26.1 MHz) to an IF frequency of 10.7 MHz.

7.7 VCO and dividers

The varactor tuned LC oscillator together with the dividers provides the LO signal for both AM and FM front-end mixers. The VCO has an operating frequency of approximately 160 MHz to 256 MHz. In FM mode the LO frequency is divided by 2 or 3. These dividers generate in-phase and quadrature-phase output signals used in the FM front-end mixer for image rejection. In weather band mode the LO signal is directly phase shifted to generate the in-phase and quadrature-phase signals. In AM mode the LO frequency is divided by 6, 8, 10, 16 or 20 depending on the selected AM band.

7.8 Tuning PLL

The tuning PLL locks the VCO frequency divided by the programmable divider ratio to the reference frequency. Due to the combination of different charge pump signals in the PLL loop filter, the loop parameters are adapted dynamically. Tuning to different RF frequencies is done by changing the programmable divider ratio. The tuning step size is selected with the reference frequency divider setting.

7.9 AM/FM IF AGC amplifier

The combined AM/FM IF AGC amplifier delivers a suitable IF signal for the ADC in the IF DSP. The maximum gain of the IF AGC amplifier can be selected via the I^2C-bus. The gain of this amplifier is automatically adapted via interfacing signals from the IF DSP. The IF AGC amplifier has three signal inputs, two for FM and one for AM. This allows the application of multiple external filters, e.g. with different bandwidths.

8. I^2C-bus protocol

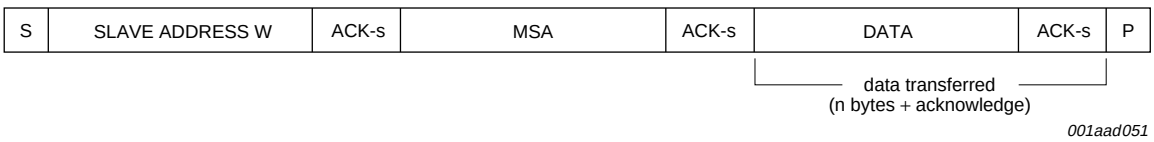


Fig 3. Write mode

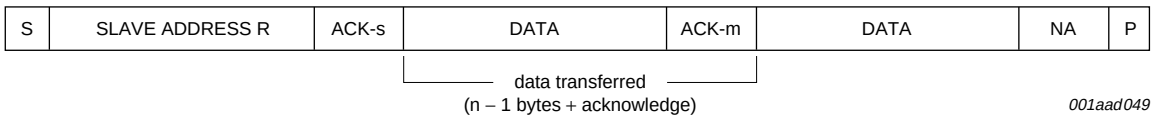


Fig 4. Read mode

Table 4. Description of I²C-bus format

Code	Description
S	START condition
Slave address W	1100 0000b for pin ADDR2 and pin ADDR1 grounded
	1100 0010b for pin ADDR2 grounded and pin ADDR1 floating
	1100 0100b for pin ADDR2 floating and pin ADDR1 grounded
	1100 0110b for pin ADDR2 and pin ADDR1 floating
Slave address R	1100 0001b for pin ADDR2 and pin ADDR1 grounded
	1100 0011b for pin ADDR2 grounded and pin ADDR1 floating
	1100 0101b for pin ADDR2 floating and pin ADDR1 grounded
	1100 0111b for pin ADDR2 and pin ADDR1 floating
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge
MSA	mode and subaddress byte
Data	data byte
P	STOP condition

8.1 Read mode

Read data is loaded into the I²C-bus register at the preceding acknowledge clock pulse.

Table 5. Read register overview

Data byte	Name	Reference
0h	TUNER	Section 8.1.1
1h	ID	Section 8.1.2

8.1.1 Read mode: data byte TUNER

Table 6. TUNER - data byte 0h bit allocation

7	6	5	4	3	2	1	0
RAGC1	RAGC0	TAS1	TAS0	-	-	-	POR

Table 7. TUNER - data byte 0h bit description

Bit	Symbol	Description
7 and 6	RAGC[1:0]	RF AGC attenuation indicator
		AM mode, PIN diode current on pin IAMAGC:
		00 = no AGC
		01 = LNA AGC
		10 = I_{AGC} < 1 mA
		11 = I_{AGC} > 1 mA
		FM mode, PIN diode current on pin IFMAGC:
		00 = < 0.1 mA
		01 = 0.1 mA to 0.5 mA
		10 = 0.5 mA to 2.5 mA
		11 = > 2.5 mA
5 and 4	TAS[1:0]	tuning action state; the signal TAS informs about internal control functions of the tuner action state machine; this way the progress of tuner actions can be monitored by the microcontroller; see Figure 8 to Figure 18
		00 = no current action
		01 = mute started and in progress at DSP
		10 = PLL tuning in progress and mute activated at DSP
		11 = PLL tuning ready and mute activated at DSP
3 to 1	-	not used
0	POR	power-on reset
		0 = normal operation
		1 = I^2C-bus data is reset to default POR state; POR is reset to logic 0 after the TEF6730A has been read out and written to via I^2C-bus at least once

8.1.2 Read mode: data byte ID

Table 8. ID - data byte 1h bit allocation

7	6	5	4	3	2	1	0
-	-	-	-	-	ID2	ID1	ID0

Table 9. ID - data byte 1h bit description

Bit	Symbol	Description
7 to 3	-	not used
2 to 0	ID[2:0]	device type identification 110 = TEF6730A

8.2 Write mode

The tuner is controlled by the I^2C-bus. After the IC address the MSA byte contains the control of the tuning action via the bits MODE[2:0] and REGC and subaddressing via bits SA[3:0] (see Figure 5).

The tuner circuit is controlled by the CONTROL register. Any data change in the CONTROL register has immediate effect and will change the operation of the tuner circuit accordingly. Transmitted I^2C-bus data is not loaded into the CONTROL register directly but loaded into a BUFFER register instead. This allows the IC to take care of tuning actions freeing the microcontroller from cumbersome controls and timings.

Controlled by a state machine, the BUFFER data will be loaded into the CONTROL register for new settings. However, at the same time the CONTROL data is loaded into the BUFFER register. This register swap action allows a fast return to the previous setting because the previous data remains available in the BUFFER register (see Figure 6 and Figure 7).

Via MODE several operational modes can be selected for the state machine. MODE offers all standard tuning actions as well as generic control for flexibility. The state machine controls the tuner by controlling the internal I^2C-bus data. Action progress is monitored by the accompanying IF DSP via the AFSAMPLE and AFHOLD lines. This way, functions like tuning mute and weak signal processing can be controlled complementary to the tuner action.

The state machine operation starts at the end of transmission (P = STOP). In case a previous action is still active, this is ignored and the new action defined by MODE is started immediately. When only the address byte is transmitted, no action is started at all (device presence test).

To minimize the I^2C-bus transmission time, only bytes that include data changes need to be written. Following the MSA byte the transmission can start at any given data byte defined by the subaddress (SA) bits.

Furthermore, when writing the buffered range either the current BUFFER data or the current CONTROL data can be used as default, controlled by the REGC bit:

- With REGC = 0, any BUFFER data that is not newly written via I^2C-bus remains unchanged. In general, the BUFFER register will contain the previous tuner setting, so this becomes default for the new setting. When only the MSA byte is transmitted defining a tuning MODE with REGC = 0, the tuner will return to its previous settings (see Figure 6).
- With REGC = 1, the BUFFER register is loaded with data from the CONTROL register first. This way, not written BUFFER data equals the CONTROL data. Since the CONTROL register contains the current tuner setting with REGC = 1, the current tuner setting is default for the new setting. When a tuning MODE action is defined with REGC = 1, the tuner will keep its current settings (CONTROL = current) for all data that is not newly written during the transmission (see Figure 7).

After power-on reset, all registers are in their default settings. The control signals for the IF DSP are set to AFSAMPLE = HIGH and AFHOLD = HIGH (i.e. mute state). Any action of the state machine will change this setting to a new one as defined by the bits MODE[2:0].

Table 10. Write mode subaddress overview

Subaddress	Name	Default	Reference
0h	CONTROL	0000 0100b	Section 8.2.2
1h	PLLM	0000 1000b	Section 8.2.3
2h	PLLL	0111 1110b	Section 8.2.4
3h	DAA	0100 0000b	Section 8.2.5
4h	AGC	1000 0000b	Section 8.2.6
5h	BAND	0010 0000b	Section 8.2.7
Fh	TEST	0000 0000b	Section 8.2.8

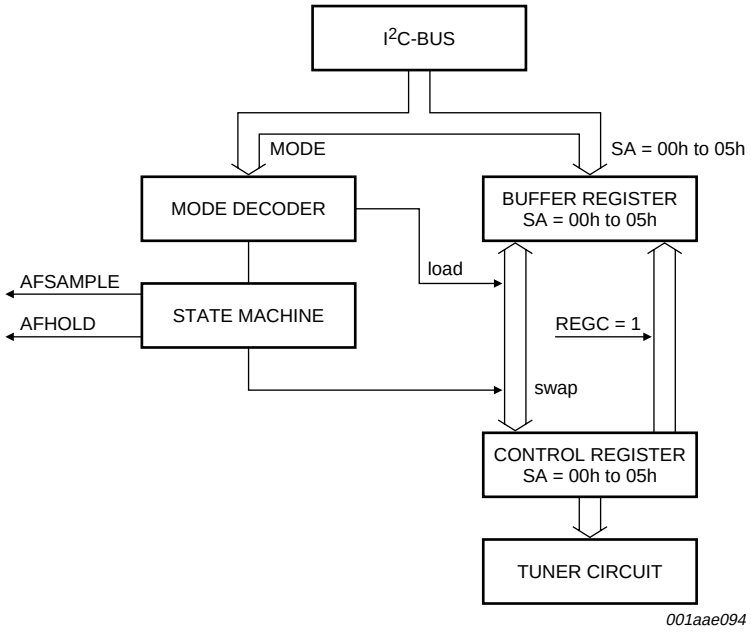


Fig 5. I²C-bus control

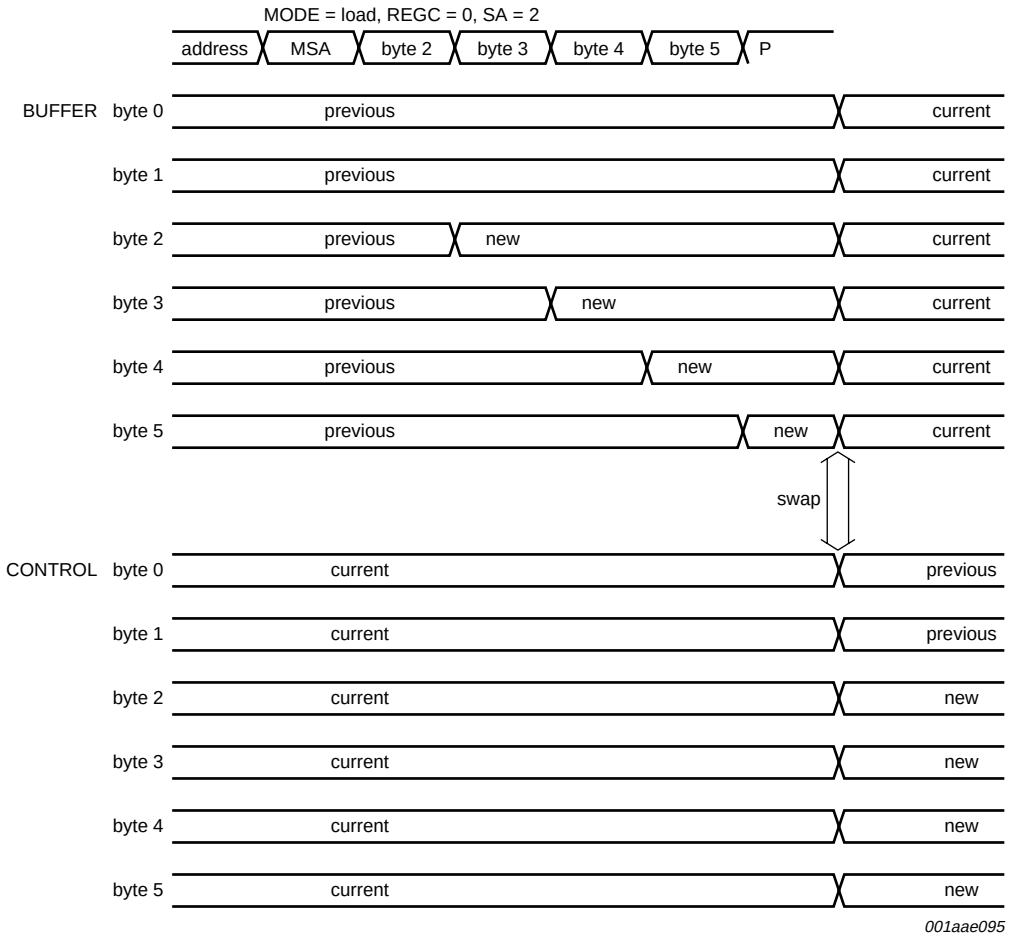


Fig 6. Write to CONTROL register with swap, REGC = 0

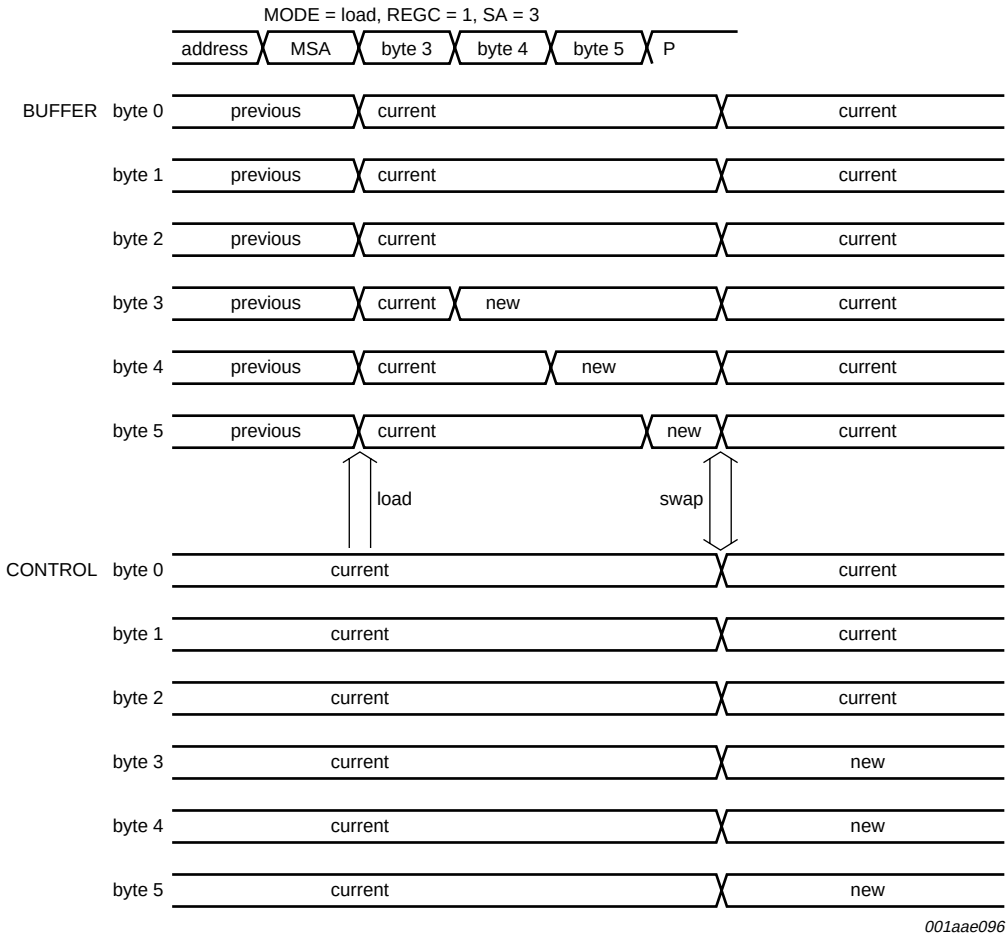


Fig 7. Write to CONTROL register with swap, REGC = 1

8.2.1 Mode and subaddress byte for write

Table 11. MSA - mode and subaddress byte bit allocation

7	6	5	4	3	2	1	0
MODE2	MODE1	MODE0	REGC	SA3	SA2	SA1	SA0

Table 12. MSA - mode and subaddress byte bit description

Bit	Symbol	Description
7 to 5	MODE[2:0]	mode; see Table 13
4	REGC	register mode
		0 = buffer mode or back mode: previous tuning data is default for new I²C-bus write (data of the BUFFER register is not changed before I²C-bus write); see Figure 6
		1 = control mode or current mode: current tuning data is default for new I²C-bus write (the BUFFER register is loaded with CONTROL register data before I²C-bus write); see Figure 7
3 to 0	SA[3:0]	subaddress; write data byte subaddress 0 to 15. The subaddress value is auto-incremented and will revert from SA = 15 to SA = 0. The auto-increment function cannot be switched off.

Table 13. Tuning action modes[1]

MODE2	MODE1	MODE0	Symbol	Description[2]
0	0	0	buffer	write BUFFER register, no state machine action, no swap
0	0	1	preset	tune to new program with 60 ms mute control; swap[3]; see Figure 8 and Figure 9
0	1	0	search	tune to new program and stay muted (for release use end mode); swap[3]; see Figure 10 and Figure 11
0	1	1	AF update	tune to AF program; check AF quality and tune back to main program; two swap operations[4]; see Figure 12 and Figure 13
1	0	0	jump	tune to AF program in minimum time; swap; see Figure 14 and Figure 15
1	0	1	check	tune to AF program and stay muted (for release use end mode); swap; see Figure 16 and Figure 17
1	1	0	load	write CONTROL register via BUFFER; no state machine action; immediate swap; see Figure 6 and Figure 7
1	1	1	end	end action; release mute; no swap; see Figure 18

[1] When the write transmission of a state machine command starts during a mute state of the state machine, the sequences of the state machine start immediately with the actions which follow the mute period in the standard sequence (see Figure 9, Figure 11, Figure 13, Figure 15 and Figure 17).

[2] References to mute are only used for better understanding. Muting is performed in the IF DSP controlled by the tuner AFHOLD and AFSAMPLE lines.

[3] In the modes preset and search the AM AGC time constant is set to fast during the period of complete mute.

[4] The AF update sequence can also be started by pulling the AFHOLD pin LOW. In this case the AF information should be loaded into the BUFFER before. LOW period for a correct AF update timing: $t_{LOW} > 20\ \mu s$. Between the end of the I²C-bus transmission and the falling edge of the AFHOLD pulse a delay of $\geq 20\ \mu s$ is necessary.

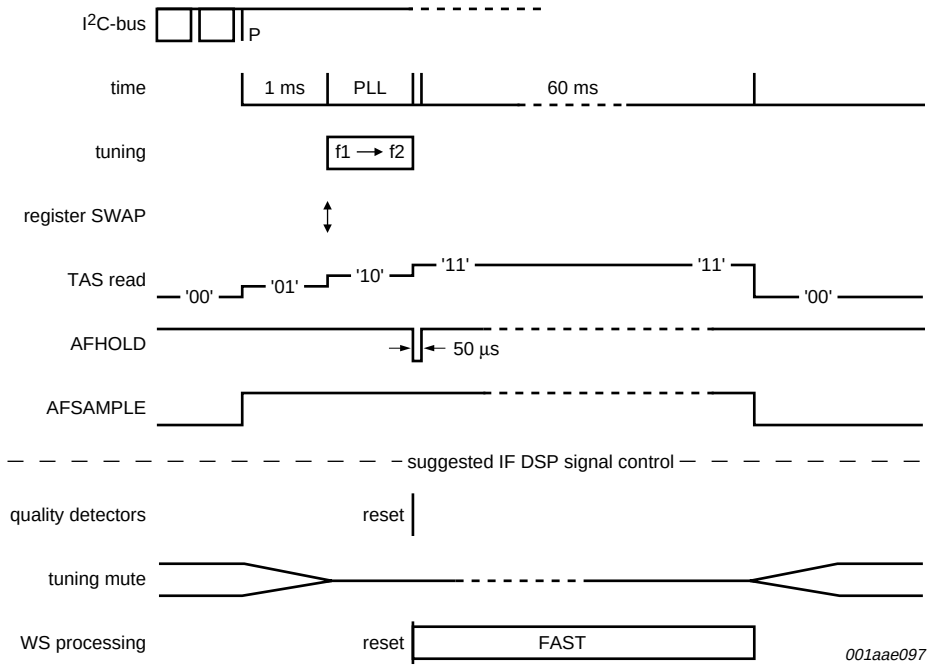


Fig 8. Preset mode

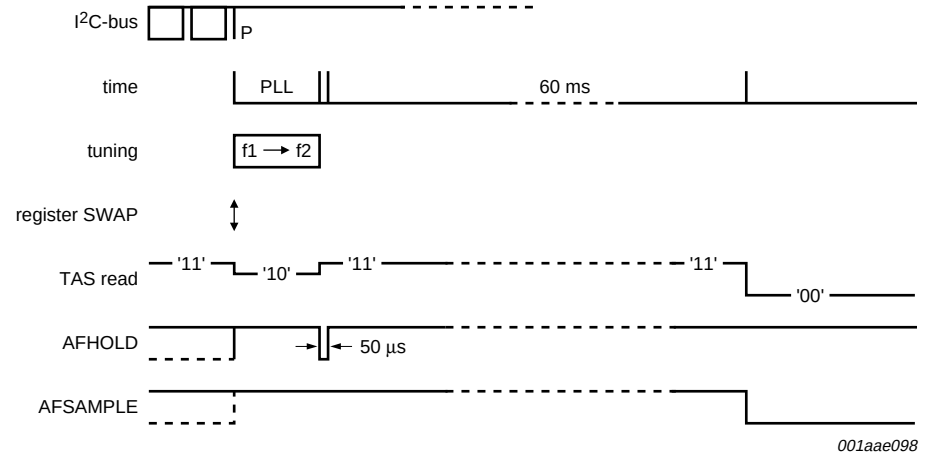


Fig 9. Preset mode, started during mute

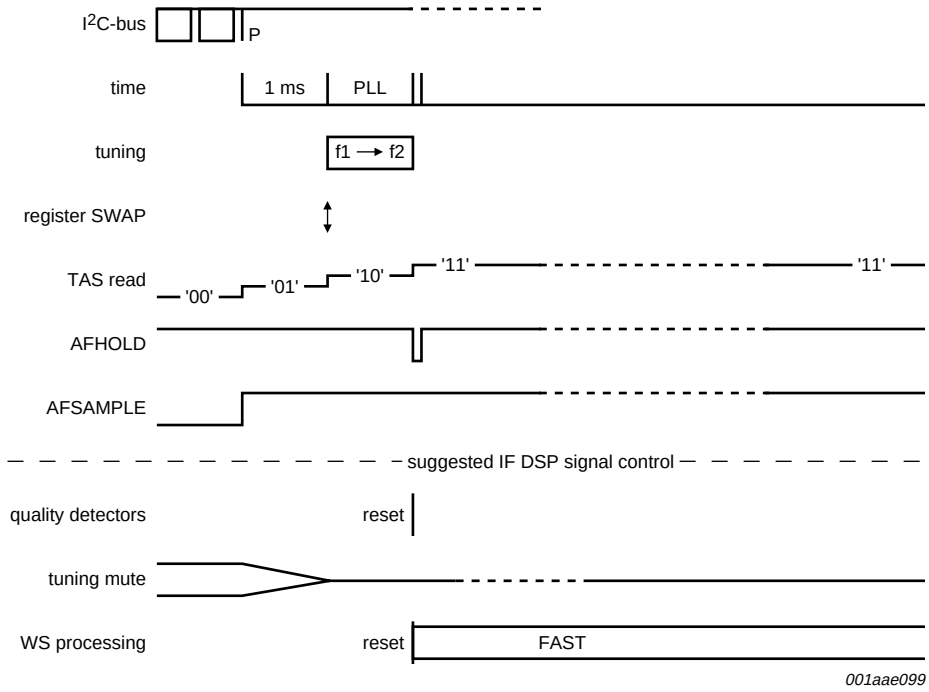


Fig 10. Search mode

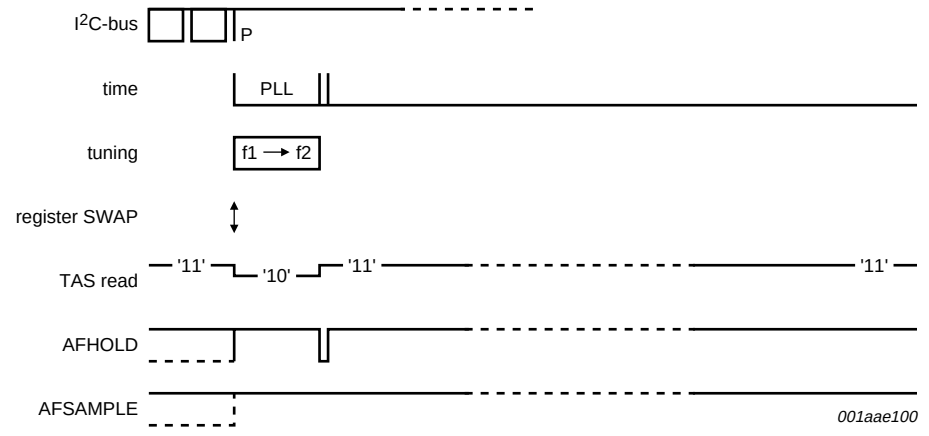


Fig 11. Search mode, started during mute

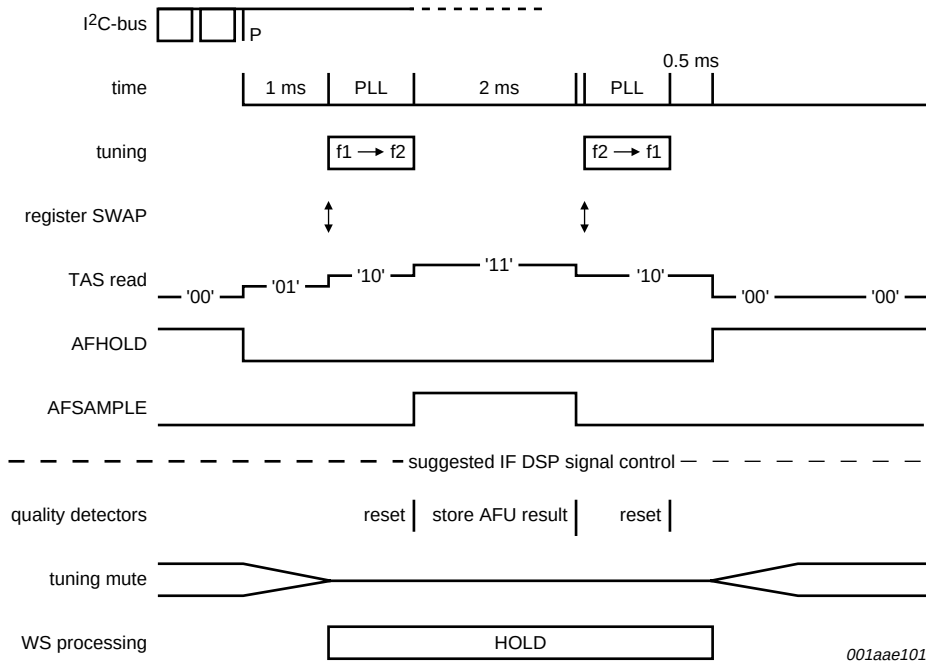


Fig 12. AF update mode

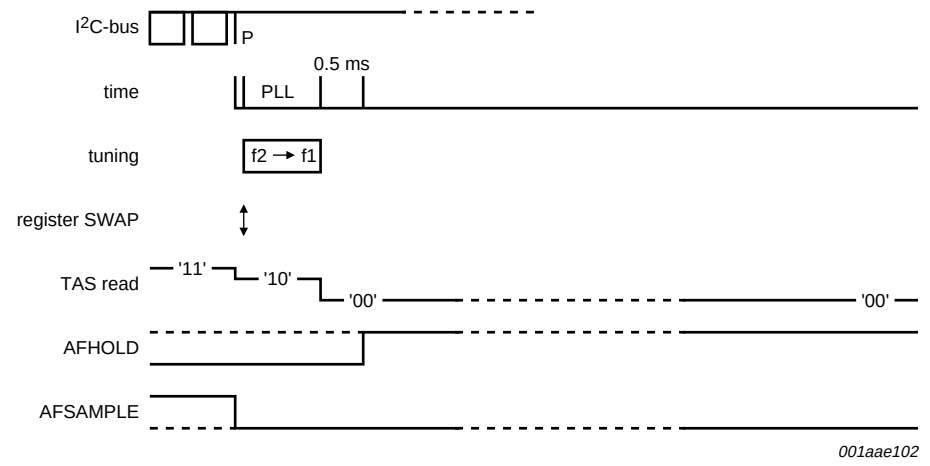


Fig 13. AF update mode, started during mute

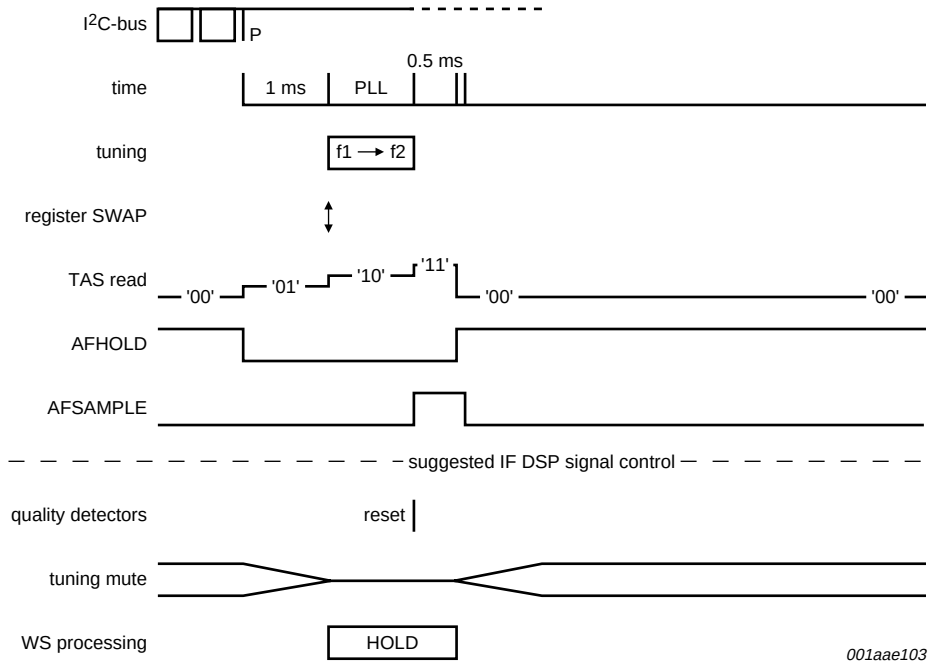


Fig 14. Jump mode

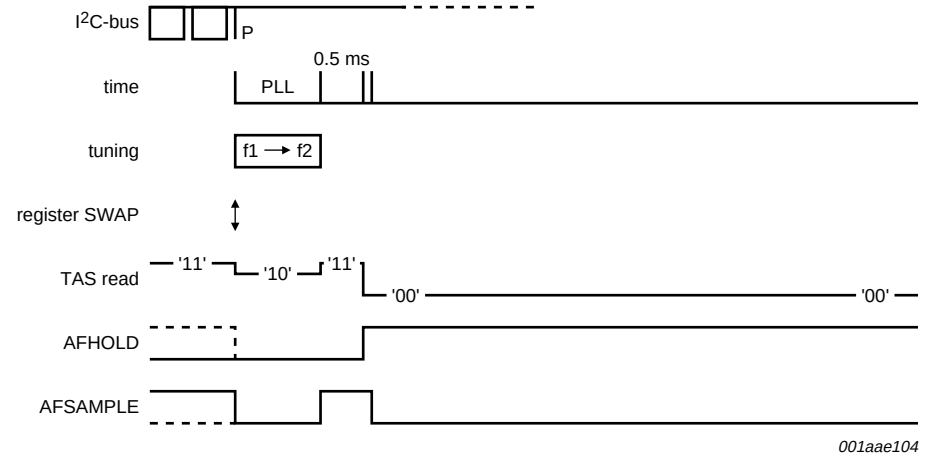


Fig 15. Jump mode, started during mute

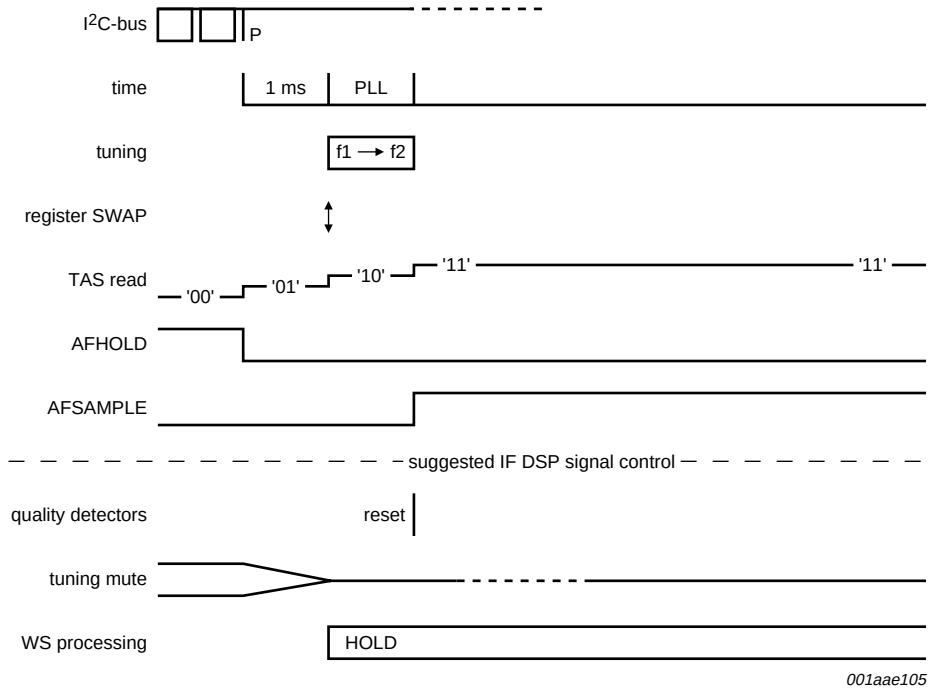


Fig 16. Check mode

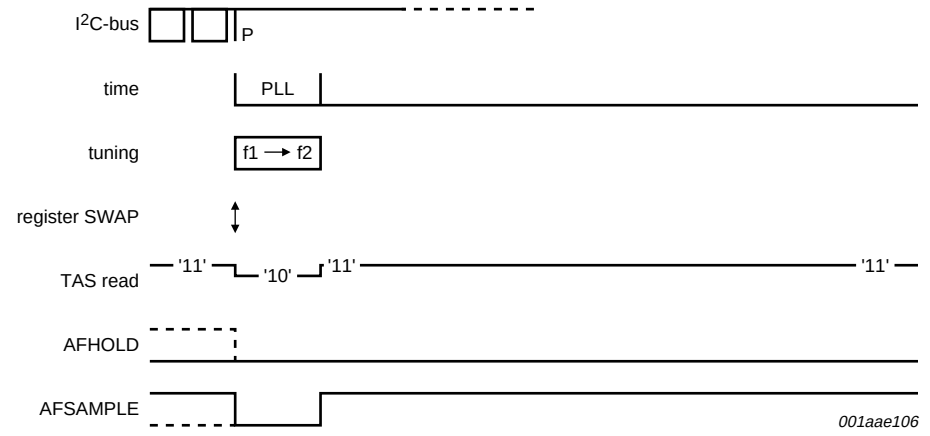


Fig 17. Check mode, started during mute

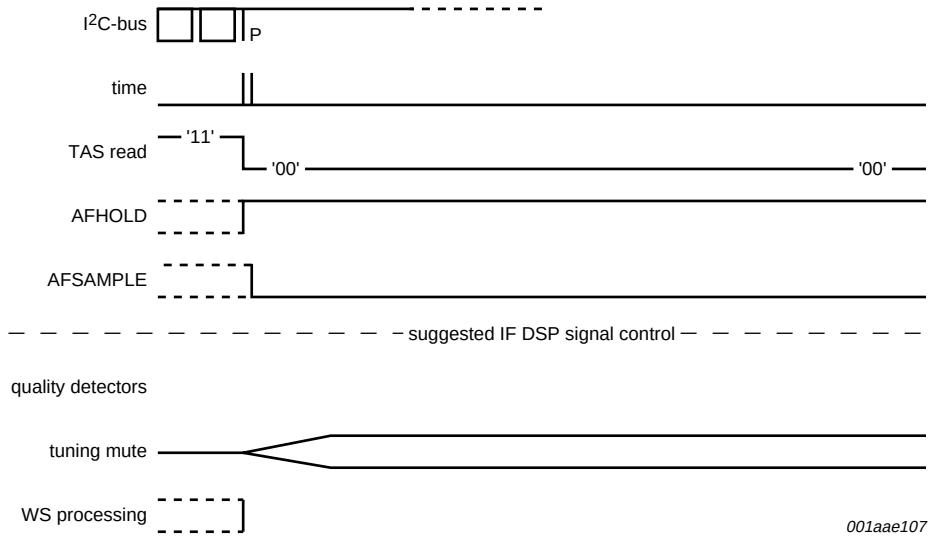


Fig 18. End mode

8.2.2 Write mode: data byte CONTROL

Table 14. CONTROL - data byte 0h bit allocation with default setting

7	6	5	4	3	2	1	0
RFGAIN	0	FLAG	IFGAIN	NBAGC1	NBAGC0	DAASW	CFSW
0		0	0	0	1	0	0

Table 15. CONTROL - data byte 0h bit description

Bit	Symbol	Description
7	RFGAIN	FM RF gain
		0 = standard gain
		1 = +6 dB added gain
6	-	not used, must be set to logic 0
5	FLAG	software port output open-collector
		0 = SWPORT pin inactive (high-impedance)
		1 = SWPORT pin active (pull-down to ground)
4	IFGAIN	IF gain
		0 = standard IF gain
		1 = increased IF gain (6 dB)
3 and 2	NBAGC[1:0]	RF AGC start level; setting of narrow band (IF) detection
		00 = 700 mV (peak value)
		01 = 560 mV (peak value)
		10 = 450 mV (peak value)
		11 = 350 mV (peak value)

Table 15. CONTROL - data byte 0h bit description *…continued*

Bit	Symbol	Description
1	DAASW	antenna DAA mode in FM
		0 = standard; DAA output voltage is controlled by V_{tune}
		1 = DAA output voltage is a fixed temperature stable voltage controlled by the DAA setting (independent of V_{tune})
0	CFSW	ceramic filter switch
		0 = CFSW1 pin active (low-impedance) and CFSW2 pin inactive (high-impedance)
		1 = CFSW2 pin active (low-impedance) and CFSW1 pin inactive (high-impedance)

8.2.3 Write mode: data byte PLLM

Table 16. PLLM - data byte 1h bit allocation with default setting

7	6	5	4	3	2	1	0
CPOFF	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8
0	0	0	0	1	0	0	0

Table 17. PLLM - data byte 1h bit description

Bit	Symbol	Description
7	CPOFF	charge pump off
		0 = standard operation
		1 = charge pump deactivated
6 to 0	PLL[14:8]	upper byte of PLL divider word

8.2.4 Write mode: data byte PLLL

Table 18. PLLL - data byte 2h bit allocation with default setting

7	6	5	4	3	2	1	0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
0	1	1	1	1	1	1	0

Table 19. PLLL - data byte 2h bit description

Bit	Symbol	Description
7 to 0	PLL[7:0]	lower byte of PLL divider word; PLL[14:0] is the divider ratio N of the VCO programmable divider; N = 1024 to 32767

8.2.5 Write mode: data byte DAA

Table 20. DAA - data byte 3h bit allocation with default setting

7	6	5	4	3	2	1	0
AGCSW	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0
0	1	0	0	0	0	0	0

Table 21. DAA - data byte 3h bit description

Bit	Symbol	Description
7	AGCSW	RF AGC switch
		0 = no drive of unused RF AGC PIN diode (FM PIN diode in AM mode or AM PIN diode in FM mode)
		1 = unused PIN diode supplied with constant current
6 to 0	DAA[6:0]	alignment of antenna circuit tuning voltage in FM mode ($0.1V_{tune}$ to $2.0V_{tune}$)

8.2.6 Write mode: data byte AGC

Table 22. AGC - data byte 4h bit allocation with default setting

7	6	5	4	3	2	1	0
SDAA3	SDAA2	SDAA1	SDAA0	WBAGC1	WBAGC0	KAGC	LODX
1	0	0	0	0	0	0	0

Table 23. AGC - data byte 4h bit description

Bit	Symbol	Description
7 to 4	SDAA[3:0]	alignment of second antenna circuit tuning voltage in FM mode ($0.7V_{DAAOUT1}$ to $1.35V_{DAAOUT1}$)
3 and 2	WBAGC[1:0]	RF AGC start level; setting of wideband (RF) detection; for AM, see Table 24 and for FM, see Table 25
1	KAGC	FM keyed AGC
		0 = keyed AGC off
		1 = keyed AGC on
0	LODX	local switch
		0 = standard operation (DX)
		1 = forced FM RF AGC attenuation (LOCAL)

Table 24. Setting of RF AGC threshold voltage for AM

WBAGC1	WBAGC0	AM output (RMS value) at LNAOUT
0	0	250 mV
0	1	200 mV
1	0	150 mV
1	1	70 mV

Table 25. Setting of RF AGC threshold voltage for FM

WBAGC1	WBAGC0	FM mixer input voltage (RMS value) at FMMIXIN
0	0	24 mV
0	1	17 mV
1	0	12 mV
1	1	9 mV

8.2.7 Write mode: data byte BAND

Table 26. BAND - data byte 5h bit allocation with default setting

7	6	5	4	3	2	1	0
BAND2	BAND1	BAND0	FREF2	FREF1	FREF0	LOINJ	FMIFIN
0	0	1	0	0	0	0	0

Table 27. BAND - data byte 5h bit description

Bit	Symbol	Description
7 to 5	BAND[2:0]	see Table 28
4 to 2	FREF[2:0]	PLL reference frequency; see Table 29
1	LOINJ	0 = high injection image suppression
		1 = low injection image suppression
0	FMIFIN	0 = FMIFAGCIN1 input is selected
		1 = FMIFAGCIN2 input is selected

Table 28. Decoding of BAND bits

BAND2	BAND1	BAND0	Divider ratio M	Receiver band
0	0	0	1	WB
0	0	1	2	FM
0	1	0	3	FM
0	1	1	6	AM
1	0	0	8	AM
1	0	1	10	AM
1	1	0	16	AM
1	1	1	20	AM

Table 29. Reference frequencies

FREF2	FREF1	FREF0	f_{ref}
0	0	0	100 kHz
0	0	1	50 kHz
0	1	0	25 kHz
0	1	1	20 kHz
1	0	0	10 kHz
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

The correct charge pump current for each reference frequency is selected automatically, see Table 30.

Table 30. Charge pump source[1]

FREF2	FREF1	FREF0	LOINJ	Charge pump current	f_{ref}
0	0	0	X	CP1	100 kHz
0	0	1	X	CP2	50 kHz
0	1	0	X	CP3	25 kHz
0	1	1	1	CP3	20 kHz
0	1	1	0	CP4	20 kHz
1	0	0	X	CP5	10 kHz

[1] X = don't care.

8.2.7.1 Tuning overview

If LOINJ = 0: $N = \frac{(f_{RF} + 10.7\ MHz) \times M}{f_{ref}}$.

If LOINJ = 1: $N = \frac{(f_{RF} - 10.7\ MHz) \times M}{f_{ref}}$.

$tuning\ step = \frac{f_{ref}}{M}$; where M is the divider ratio of the VCO frequency for AM mixer and FM mixer $M = \frac{f_{VCO}}{f_{mixer}}$.

Table 31. Standard tuner settings

Broadcast band	BAND2	BAND1	BAND0	M	FREF2	FREF1	FREF0	f_{ref}	LOINJ	Tuning step
Europe FM and US FM	0	0	1	2	0	0	0	100 kHz	0	50 kHz
Japan FM	0	1	0	3	0	0	0	100 kHz	1	33.3 kHz
East Europe FM (OIRT FM)	0	1	0	3	0	1	1	20 kHz	1	6.67 kHz
WB FM	0	0	0	1	0	1	0	25 kHz	0	25 kHz
AM MW and LW	1	1	1	20	0	1	1	20 kHz	0	1 kHz
AM SW 120 m to 60 m	1	1	0	16	1	0	0	10 kHz	0	0.625 kHz
AM SW 49 m to 22 m	1	0	1	10	1	0	0	10 kHz	0	1 kHz
AM SW 25 m to 15 m	1	0	0	8	1	0	0	10 kHz	0	1.25 kHz
AM SW 16 m to 11 m	0	1	1	6	1	0	0	10 kHz	0	1.67 kHz

8.2.8 Write mode: data byte TEST

Table 32. TEST - data byte Fh bit allocation with default setting (not buffered)[1]

7	6	5	4	3	2	1	0
0	0	0	0	TEST3	TEST2	TEST1	TEST0
				0	0	0	0

[1] The test control byte is for internal use only.

9. Limiting values

Table 33. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage	on pins V_{CC}, $V_{CC(PLL)}$, $V_{CC(VCO)}$, $V_{CC(RF)}$, $V_{CC(IF)}$, FMMIXOUT1, FMMIXOUT2, AMMIXOUT1 and AMMIXOUT2		–0.3	+10	V
ΔV_{CCAn}	voltage difference between any analog supply pins			–0.3	+0.3	V
V_{SCL}	voltage on pin SCL			–0.3	+5.5	V
V_{SDA}	voltage on pin SDA			–0.3	+5.5	V
V_i	input voltage	on pins ADDR1 and ADDR2	[1]	–0.3	+5.5	V
V_o	output voltage	on pins AFHOLD and AFSAMPLE		–0.3	+5.5	V
		on pin SWPORT		–0.3	+10	V
V_n	voltage on any other pin			–0.3	V_{CCA} + 0.3	V
P_{tot}	total power dissipation			-	1100	mW
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature	soldered exposed die pad				
		subjective functionality		–40	+105	°C
		full functionality		–40	+85	°C
V_{esd}	electrostatic discharge voltage	on all pins except pin $V_{CC(VCO)}$	[2]	–2000	+2000	V
			[3]	–500	+500	V
		on pin $V_{CC(VCO)}$	[4]	–1000	+2000	V
			[3]	–500	+500	V

[1] The maximum voltage must be less than V_{CCA}.

[2] Human body model: Class 2 according to JESD22-A114C.01.

[3] Charge device model: Class 3 according to JESD22-C101C.

[4] Human body model: Class 1C according to JESD22-A114C.01.

10. Thermal characteristics

Table 34. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	29.6	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		17.5	K/W

11. Static characteristics

Table 35. Static characteristics

V_{CCA} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{CCA}	analog supply voltage	on pins V_{CC}, $V_{CC(PLL)}$, $V_{CC(VCO)}$, $V_{CC(RF)}$, $V_{CC(IF)}$, FMMIXOUT1, FMMIXOUT2, AMMIXOUT1 and AMMIXOUT2	8	8.5	9	V
Current in FM mode						
$I_{CC(RF)}$	RF supply current	T_{amb} = –40 °C	-	14	-	mA
		T_{amb} = 25 °C	-	15	-	mA
		T_{amb} = 85 °C	-	16	-	mA
$I_{CC(PLL)}$	PLL supply current	T_{amb} = –40 °C	-	7.9	-	mA
		T_{amb} = 25 °C	-	7.6	-	mA
		T_{amb} = 85 °C	-	7.2	-	mA
$I_{CC(VCO)}$	VCO supply current	T_{amb} = –40 °C	-	3.8	-	mA
		T_{amb} = 25 °C	-	3.6	-	mA
		T_{amb} = 85 °C	-	3.5	-	mA
I_{CC}	supply current	T_{amb} = –40 °C	-	23	-	mA
		T_{amb} = 25 °C	-	21.5	-	mA
		T_{amb} = 85 °C	-	19	-	mA
$I_{CC(IFAGC)}$	IF AGC supply current	T_{amb} = –40 °C	-	26	-	mA
		T_{amb} = 25 °C	-	26	-	mA
		T_{amb} = 85 °C	-	26	-	mA
$I_{FMMIXOUT1}$	current on pin FMMIXOUT1	T_{amb} = –40 °C	-	5.3	-	mA
		T_{amb} = 25 °C	-	5.8	-	mA
		T_{amb} = 85 °C	-	6.1	-	mA
$I_{FMMIXOUT2}$	current on pin FMMIXOUT2	T_{amb} = –40 °C	-	5.3	-	mA
		T_{amb} = 25 °C	-	5.8	-	mA
		T_{amb} = 85 °C	-	6.1	-	mA
$I_{CC(tot)}$	total supply current		-	85.3	-	mA
Current in AM mode						
$I_{CC(RF)}$	RF supply current	T_{amb} = –40 °C	-	39.5	-	mA
		T_{amb} = 25 °C	-	39	-	mA
		T_{amb} = 85 °C	-	38	-	mA
$I_{CC(PLL)}$	PLL supply current	T_{amb} = –40 °C	-	7.9	-	mA
		T_{amb} = 25 °C	-	7.6	-	mA
		T_{amb} = 85 °C	-	7.2	-	mA
$I_{CC(VCO)}$	VCO supply current	T_{amb} = –40 °C	-	3.8	-	mA
		T_{amb} = 25 °C	-	3.6	-	mA
		T_{amb} = 85 °C	-	3.5	-	mA

Table 35. Static characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	T_{amb} = –40 °C	-	21.5	-	mA
		T_{amb} = 25 °C	-	21	-	mA
		T_{amb} = 85 °C	-	20	-	mA
$I_{CC(IFAGC)}$	IF AGC supply current	T_{amb} = –40 °C	-	33	-	mA
		T_{amb} = 25 °C	-	32.5	-	mA
		T_{amb} = 85 °C	-	32	-	mA
$I_{AMMIXOUT1}$	current on pin AMMIXOUT1	T_{amb} = –40 °C	-	6	-	mA
		T_{amb} = 25 °C	-	5.5	-	mA
		T_{amb} = 85 °C	-	5	-	mA
$I_{AMMIXOUT2}$	current on pin AMMIXOUT2	T_{amb} = –40 °C	-	6	-	mA
		T_{amb} = 25 °C	-	5.5	-	mA
		T_{amb} = 85 °C	-	5	-	mA
$I_{CC(tot)}$	total supply current		-	114.7	-	mA

12. Dynamic characteristics

Table 36. Dynamic characteristics

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference frequency							
External reference frequency, circuit inputs: pins FREF1 and FREF2							
f_{ext}	external frequency			-	100	-	kHz
C/N	carrier-to-noise ratio	required from reference source; f_{ext} = 100 kHz; Δf = 10 kHz		115	-	-	dBc/√Hz
$I_{i(ext)(min)(M)}$	peak minimum external input current	square wave signal	[1]	-	-	200	µA
$I_{i(ext)(max)(M)}$	peak maximum external input current	square wave signal	[1]	750	-	-	µA
$I_{cm(ext)}$	external common-mode current	from each pin to GND		–50	-	+50	µA
R_i	input resistance			-	5	10	Ω
V_{cm}	common-mode voltage	measured between each pin to GND		1.0	1.2	1.4	V
Tuning system; see Table 28, Table 29, Table 30 and Table 31							
Voltage controlled oscillator							
$f_{VCO(min)}$	minimum VCO frequency		[2]	-	-	130	MHz
		application according to Figure 25	[2]	-	-	159.9	MHz
$f_{VCO(max)}$	maximum VCO frequency		[2]	256	-	-	MHz
C/N	carrier-to-noise ratio	f_{VCO} = 200 MHz; Δf = 10 kHz; Q = 30		94	98	-	dBc/√Hz

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Δf	frequency deviation	caused by ripple on supply voltage; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 50 mV (RMS); f_{VCO} = 200 MHz; standard FM	-	2	-	Hz
Charge pump: pin CPOUT; see Table 30						
$I_{sink(CP1)}$	CP1 sink current	V_{CPOUT} = 0.5 V to $V_{CC(PLL)}$ − 1.3 V	130	180	240	µA
$I_{source(CP1)}$	CP1 source current	V_{CPOUT} = 0.5 V to $V_{CC(PLL)}$ − 1.3 V	−240	−180	−130	µA
$I_{sink(CP2)}$	CP2 sink current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 1.5 V	270	360	480	µA
$I_{source(CP2)}$	CP2 source current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 1.5 V	−480	−360	−270	µA
$I_{sink(CP3)}$	CP3 sink current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V	580	780	1050	µA
$I_{source(CP3)}$	CP3 source current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V	−1050	−780	−580	µA
$I_{sink(CP4)}$	CP4 sink current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V	1040	1400	1900	µA
$I_{source(CP4)}$	CP4 source current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V	−1900	−1400	−1040	µA
$I_{sink(CP5)}$	CP5 sink current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V	1630	2200	2970	µA
$I_{source(CP5)}$	CP5 source current	V_{CPOUT} = 0.7 V to $V_{CC(PLL)}$ − 0.7 V	−2970	−2200	−1630	µA
Charge pump: pin VTUNE						
$I_{o(sink)}$	output sink current	V_{tune} = 0.9 V to $V_{CC(PLL)}$ − 0.7 V	2070	2800	3780	µA
$I_{o(source)}$	output source current	V_{tune} = 0.9 V to $V_{CC(PLL)}$ − 0.7 V	−3780	−2800	−2070	µA
Timings						
t_{tune}	tuning time	Europe FM and US FM band; f_{ref} = 100 kHz; f_{RF} = 87.5 MHz to 108 MHz	-	0.75	1	ms
		AM MW band; f_{ref} = 20 kHz; f_{RF} = 0.53 MHz to 1.7 MHz	-	-	10	ms
$t_{upd(AF)}$	AF update time	cycle time for inaudible AF update including 1 ms mute start and 1 ms mute release time	-	6	6.5	ms
Antenna Digital Auto Alignment (DAA)						
DAA1: pin DAAOUT1[3]						
$G_{conv(DAA)}$	DAA conversion gain		0.1	-	2	

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_o	output voltage	FM mode; DAASW = 0				
		minimum value	-	-	0.6	V
		maximum value	$V_{CC(PLL)}$ – 0.6	-	-	V
		FM mode; DAASW = 1; independent of tuning voltage				
		minimum value; data byte DAA bits DAA[6:0] = 000 0000	-	-	0.6	V
		maximum value; data byte DAA bits DAA[6:0] = 111 1111	$V_{CC(PLL)}$ – 0.6	-	-	V
		AM mode; independent of tuning voltage				
		minimum value; data byte DAA bits DAA[6:0] = 000 0000	-	-	0.6	V
		maximum value; data byte DAA bits DAA[6:0] = 111 1111	$V_{CC(PLL)}$ – 0.6	-	-	V
$V_{n(o)}$	output noise voltage	data byte DAA bits DAA[6:0] = 100 0000; FM mode; V_{tune} = 4 V with frequency range from 300 Hz to 22 kHz	-	30	100	µV
$\Delta V_{o(T)}$	output voltage deviation over temperature	T_{amb} = –40 °C to +85 °C; data byte DAA bits DAA[6:0] = 100 0000	–30	-	+30	mV
$\Delta V_{o(step)}$	step output voltage tolerance	n = 0 to 127; FM mode; V_{tune} = 4 V	$–0.5V_{LSB}$	0	$+0.5V_{LSB}$	
ΔV_o	output voltage deviation	V_{tune} = 4 V; I_{load} = 50 µA	$–V_{LSB}$	-	$+V_{LSB}$	
		V_{tune} = 4 V; I_{load} = –50 µA	$–V_{LSB}$	-	$+V_{LSB}$	
$t_{s(o)}$	output settling time	$V_{DAAOUT1}$ = 0.2 V to 8.25 V; C_L = 270 pF	-	30	60	µs
α_{ripple}	ripple rejection	$V_{CC(ripple)}$ / V_o; data byte DAA bits DAA[6:0] = 101 0101; FM mode; V_{tune} = 4 V; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 100 mV	-	40	-	dB
DAA2: pin DAAOUT2[4]						
$G_{conv(DAA)}$	DAA conversion gain		0.7	-	1.35	
V_o	output voltage	AM mode and FM mode				
		minimum value	-	-	0.6	V
		maximum value	$V_{CC(PLL)}$ – 0.8	-	-	V
$V_{n(o)}$	output noise voltage	data byte AGC bits SDAA[3:0] = 1000; FM mode; $V_{DAAOUT1}$ = 4 V with frequency range from 300 Hz to 22 kHz	-	30	100	µV

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{o(T)}$	output voltage deviation over temperature	T_{amb} = −40 °C to +85 °C; data byte AGC bits SDAA[3:0] = 1000	−30	-	+30	mV
$\Delta V_{o(step)}$	step output voltage tolerance	n = 0 to 15; FM mode; $V_{DAAOUT1}$ = 4 V	$-0.5V_{LSB}$	0	$+0.5V_{LSB}$	
ΔV_o	output voltage deviation	$V_{DAAOUT1}$ = 4 V; I_{load} = 50 µA	$-V_{LSB}$	-	$+V_{LSB}$	
		$V_{DAAOUT1}$ = 4 V; I_{load} = −50 µA	$-V_{LSB}$	-	$+V_{LSB}$	
$t_{s(o)}$	output settling time	$V_{DAAOUT1}$ = 4 V; $V_{DAAOUT2}$ = 2.8 V to 5.4 V; C_L = 270 pF	-	20	30	µs
α_{ripple}	ripple rejection	$V_{CC(ripple)}$ / $V_{DAAOUT1}$; data byte AGC bits SDAA[3:0] = 1010; FM mode; $V_{DAAOUT1}$ = 4 V; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 100 mV	-	50	-	dB
AM channel						
AM RF AGC wideband detector (average detector): pin LNAOUT						
$V_{LNAOUT(RMS)}$	RMS voltage on pin LNAOUT	start level of wideband AGC; R_L = 430 Ω (load at pin LNAOUT); m = 0.3; see Table 24 and Table 25				
		data byte AGC bits WBAGC[1:0] = 00	175	250	350	mV
		data byte AGC bits WBAGC[1:0] = 01	140	200	280	mV
		data byte AGC bits WBAGC[1:0] = 10	105	150	210	mV
		data byte AGC bits WBAGC[1:0] = 11	49	70	98	mV
AM RF AGC narrow-band detector: pins IFOUT1 and IFOUT2						
$V_{o(IFOUT)(M)}$	peak output voltage between pin IFOUT1 and pin IFOUT2	start level of narrow-band AGC; data byte CONTROL bit IFGAIN = 0; $V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW; see Table 15				
		data byte CONTROL bits NBAGC[1:0] = 00	490	700	980	mV
		data byte CONTROL bits NBAGC[1:0] = 01	390	560	780	mV
		data byte CONTROL bits NBAGC[1:0] = 10	315	450	630	mV
		data byte CONTROL bits NBAGC[1:0] = 11	245	350	490	mV
AM LNA and AGC						
Input: pin LNAIN; output: pin LNAOUT						
R_i	input resistance		0.9	1.3	1.8	MΩ

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance			-	46	69	pF
G_m	transconductance gain	I_o / V_i		36	52	74	mA/V
$\Delta G_{m(T)}$	transconductance gain deviation over temperature	T_{amb} = −40 °C to +85 °C; see Figure 19		-	-	-	dB
IP3	third-order intercept point	R_L = 430 Ω (load at pin LNAOUT)		111	114	-	dBµV
IP2	second-order intercept point	R_L = 430 Ω (load at pin LNAOUT)		120	129	-	dBµV
$V_{n(i)(eq)}$	equivalent input noise voltage	C_{source} = 110 pF; R_L = 430 Ω (load at pin LNAOUT)					
		f_{RF} = 1 MHz		-	1.1	1.55	nV/√Hz
		f_{RF} = 144 kHz		-	2.55	3.55	nV/√Hz
R_o	output resistance			80	115	165	Ω
C_o	output capacitance	in series with output resistance		-	22	33	pF
$V_{o(p-p)(max)}$	maximum peak-to-peak output voltage			-	2.2	-	V
ΔG_{AGC}	AGC gain range			8	11	14	dB
RF PIN diode AGC current generator output: pin IAMAGC							
ΔG_{AGC}	AGC gain range	f_{RF} = 1 MHz; dummy aerial 15 pF / 60 pF		-	50	-	dB
V_{IAMAGC}	voltage on pin IAMAGC	PIN diode drive DC voltage		2.2	-	V_{CCA}	V
$I_{sink(max)}$	maximum sink current	V_{IAMAGC} = 2.2 V	[5]	10	-	-	mA
I_{sink}	sink current	FM mode; data byte DAA bit AGCSW = 1		0.6	0.9	1.4	mA
		FM mode; data byte DAA bit AGCSW = 0		-	-	100	nA
AM mixer (IF = 10.7 MHz)							
Mixer input: pins AMMIXIN and AMMIXDEC							
R_i	input resistance		[6]	40	-	-	kΩ
C_i	input capacitance		[6]	-	3	4.5	pF
$V_{i(max)}$	maximum input voltage	on pin AMMIXIN; 1 dB compression point of $V_{MIXOUT1-MIXOUT2}$; m = 0		500	-	-	mV
Mixer output: pins AMMIXOUT1 and AMMIXOUT2							
R_o	output resistance		[7]	100	-	-	kΩ
C_o	output capacitance		[7]	-	4	7	pF
$V_{o(p-p)(max)}$	maximum peak-to-peak output voltage			12	15	-	V
$G_{m(conv)}$	conversion transconductance gain	I_o / V_i		1.8	2.4	3.2	mA/V

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	T_{amb} = −40 °C to +85 °C; see Figure 20	-	-	-	dB
IP3	third-order intercept point	R_L = 2.6 kΩ (AC load between output pins); Δf = 300 kHz	135	138	-	dBµV
IP2	second-order intercept point	R_L = 2.6 kΩ (AC load between output pins)	-	170	-	dBµV
$V_{n(i)(eq)}$	equivalent input noise voltage	band limited noise; R_{source} = 750 Ω; noise of R_{source} included; R_L = 2.6 kΩ (AC load between output pins)	-	7.2	10	nV/√Hz
NF	noise figure		-	6.2	9	dB
FM channel						
FM RF AGC (FM distance mode; data byte AGC bit LODX = 0)						
Input: pins FMMIXIN1 and FMMIXIN2[8]						
$V_{i(FMMIXIN)(RMS)}$	RMS input voltage between pin FMMIXIN1 and pin FMMIXIN2	start level of wideband AGC; keyed AGC off; data byte AGC bit KAGC = 0; see Table 24 and Table 25				
		data byte AGC bits WBAGC[1:0] = 11	5	9	15	mV
		data byte AGC bits WBAGC[1:0] = 10	7	12	19	mV
		data byte AGC bits WBAGC[1:0] = 01	10	17	27	mV
		data byte AGC bits WBAGC[1:0] = 00	14	24	38	mV
		start level of wideband AGC; keyed AGC on; data byte AGC bit KAGC = 1; $V_{KAGC} > V_{th(KAGC)}$				
		data byte AGC bits WBAGC[1:0] = 11	19	30	48	mV
		data byte AGC bits WBAGC[1:0] = 10	21	33	52	mV
		data byte AGC bits WBAGC[1:0] = 01	24	38	60	mV
		data byte AGC bits WBAGC[1:0] = 00	28	45	71	mV

Table 36. Dynamic characteristics *…continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM RF AGC narrow-band detector: pins IFOUT1 and IFOUT2						
$V_{o(IFOUT)(M)}$	peak output voltage between pin IFOUT1 and pin IFOUT2	start level of narrow-band AGC; data byte CONTROL bit IFGAIN = 0; $V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW; see Table 15				
		data byte CONTROL bits NBAGC[1:0] = 00	490	700	980	mV
		data byte CONTROL bits NBAGC[1:0] = 01	390	560	780	mV
		data byte CONTROL bits NBAGC[1:0] = 10	315	450	630	mV
		data byte CONTROL bits NBAGC[1:0] = 11	245	350	490	mV
PIN diode drive output: pin IFMAGC						
$I_{source(max)}$	maximum source current	V_{TFMAGC} = V_{IFMAGC} + 1.4 V; data byte AGC bit KAGC = 0	–16	–10	–7	mA
$I_{sink(max)}$	maximum sink current	at AGC decay; V_{TFMAGC} = V_{IFMAGC}; data byte AGC bit KAGC = 0	7	10	16	mA
I_{source}	source current	AM mode; data byte DAA bit AGCSW = 1	-	–1.2	-	mA
		AM mode; data byte DAA bit AGCSW = 0	-	0	-	mA
		data byte AGC bit LODX = 1 (FM local)	–0.75	–0.5	–0.35	mA
V_{IFMAGC}	voltage on pin IFMAGC	voltage at PIN diode drive output; $V_{FMMIXIN1} < V_{th}$	-	100	300	mV
$V_{th(KAGC)}$	threshold voltage on pin KAGC	threshold level voltage for narrow-band AGC (keyed AGC); data byte AGC bit KAGC = 1; see Table 15 and Table 23	500	950	1400	mV
FM mixer (IF = 10.7 MHz)						
FM RF input: pins FMMIXIN1 and FMMIXIN2[8]						
$V_{i(RF)(max)}$	maximum RF input voltage	1 dB compression point of FM mixer output voltage	75	100	-	mV
$V_{n(i)(eq)}$	equivalent input noise voltage	R_{source} = 500 Ω; noise of R_{source} included; R_L = 2.6 kΩ (on output pins FMMIXOUT1 and FMMIXOUT2)				
		RFGAIN = 0	-	4.7	6.4	nV/√Hz
		RFGAIN = 1	-	4.2	-	nV/√Hz
R_i	input resistance	RFGAIN = 0	3	3.8	4.7	kΩ
		RFGAIN = 1	1.6	2.0	2.5	kΩ

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance		-	2	4	pF
$G_{m(conv)}$	conversion transconductance gain	I_o / V_i; RF gain 1; data byte PLLM bit RFGAIN = 0	12	18	25	mA/V
		I_o / V_i; RF gain 2; data byte PLLM bit RFGAIN = 1	24	36	50	mA/V
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	T_{amb} = −40 °C to +85 °C; see Figure 21	-	-	-	dB
NF	noise figure	R_{source} = 500 Ω; T_{amb} = 25 °C				
		RFGAIN = 0	-	4.2	5.7	dB
		RFGAIN = 1	-	3.2	4.7	dB
IP3	third-order intercept point	RFGAIN = 0	117	123	-	dBµV
		RFGAIN = 1	108	114	-	dBµV
IRR	image rejection ratio	$V_{o(wanted)}$ / $V_{o(image)}$; $f_{RF(wanted)}$ = 87.5 MHz; $f_{RF(image)}$ = 108.9 MHz	25	40	-	dB
Output: pins FMMIXOUT1 and FMMIXOUT2[9]						
R_o	output resistance		100	-	-	kΩ
C_o	output capacitance		-	4	6	pF
$V_{o(p-p)(max)}$	maximum peak-to-peak output voltage		4.5	5.6	-	V
FM weather band input: pins WXMIXIN and WXMIXDEC						
$G_{m(conv)}$	conversion transconductance gain	I_o / V_i	10	15	21	mA/V
$\Delta G_{m(conv)(T)}$	conversion transconductance gain deviation over temperature	T_{amb} = −40 °C to +85 °C; see Figure 22	-	-	-	dB
R_i	input resistance		-	5.1	-	kΩ
C_i	input capacitance		-	2	4	pF
NF	noise figure	R_{source} = 300 Ω	-	3.5	5	dB
IP3	third-order intercept point		-	116	-	dBµV
IRR	image rejection ratio	$V_{o(wanted)}$ / $V_{o(image)}$; $f_{RF(wanted)}$ = 162.475 MHz; $f_{RF(image)}$ = 183.875 MHz	20	33	-	dB
IF AGC amplifier						
AM mode; inputs: pins AMIFAGCIN and IFAGCDEC[10]; outputs: pins IFOUT1 and IFOUT2[11]						
R_i	input resistance		-	100	-	kΩ
C_i	input capacitance		-	5	7	pF
R_o	output resistance		120	210	290	Ω

Table 36. Dynamic characteristics *…continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G	gain	data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	21.2	24.2	27.2	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	15.2	18.2	21.2	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	9.2	12.2	15.2	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	3.2	6.2	9.2	dB
		data byte CONTROL bit IFGAIN = 1				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	27.2	30.2	33.2	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	21.2	24.2	27.2	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	15.2	18.2	21.2	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	9.2	12.2	15.2	dB
NF	noise figure	R_{source} = 300 Ω; data byte CONTROL bit IFGAIN = 0; $V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	-	12.9	16	dB
ΔIM3	third-order intermodulation distance	two output signals at 35 kHz frequency distance; differential output level of 200 mV; data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	77	83	-	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	77	83	-	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	77	83	-	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	74	80	-	dB

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(max)(M)}$	peak maximum input voltage	1 dB compression point of IF AGC amplifier output voltage; data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	45	-	-	mV
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	90	-	-	mV
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	180	-	-	mV
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	360	-	-	mV
FM mode; inputs: pins FMIFAGCIN1 and IFAGCDEC[12]; outputs: pins IFOUT1 and IFOUT2[11]						
R_i	input resistance		-	330	-	Ω
C_i	input capacitance		-	5	7	pF
R_o	output resistance		120	210	290	Ω
G	gain	data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	28	31	34	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	22	25	28	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	16	19	22	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	10	13	16	dB
		data byte CONTROL bit IFGAIN = 1				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	34	37	40	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	28	31	34	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	22	25	28	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	16	19	22	dB
NF	noise figure	R_{source} = 300 Ω; data byte CONTROL bit IFGAIN = 0; $V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	-	6.9	8.5	dB
IP3	third-order intercept point	data byte CONTROL bit IFGAIN = 0	110	115	-	dBµV

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(max)(M)}$	peak maximum input voltage	1 dB compression point of IF AGC amplifier output voltage; data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	20	-	-	mV
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	40	-	-	mV
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	80	-	-	mV
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	160	-	-	mV
FM mode; inputs: pins FMIFAGCIN2 and IFAGCDEC[13]; outputs: pins IFOUT1 and IFOUT2[11]						
R_i	input resistance		-	330	-	Ω
C_i	input capacitance		-	5	7	pF
G	gain	data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	28	31	34	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	22	25	28	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	16	19	22	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	10	13	16	dB
		data byte CONTROL bit IFGAIN = 1				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	34	37	40	dB
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	28	31	34	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	22	25	28	dB
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	16	19	22	dB
NF	noise figure	R_{source} = 300 Ω; data byte CONTROL bit IFGAIN = 0; $V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	-	6.9	8.5	dB
IP3	third-order intercept point	data byte CONTROL bit IFGAIN = 0	110	115	-	dBµV

Table 36. Dynamic characteristics *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(max)(M)}$	peak maximum input voltage	1 dB compression point of IF AGC amplifier output voltage; data byte CONTROL bit IFGAIN = 0				
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = LOW	20	-	-	mV
		$V_{IFAGCMSB}$ = LOW; $V_{IFAGCLSB}$ = HIGH	40	-	-	mV
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = HIGH	80	-	-	mV
		$V_{IFAGCMSB}$ = HIGH; $V_{IFAGCLSB}$ = LOW	160	-	-	mV
Digital inputs and outputs						
Input: pins IFAGCMSB and IFAGCLSB						
V_{IL}	LOW-level input voltage		-	-	0.9	V
V_{IH}	HIGH-level input voltage		1.5	-	-	V
Output: pin AFHOLD						
$I_{sink(max)}$	maximum sink current	AFHOLD = LOW; V_o = 0.4 V	1.0	-	-	mA
Output: pin AFSAMPLE						
$I_{sink(max)}$	maximum sink current	AFSAMPLE = LOW; V_o = 0.4 V	1.0	-	-	mA
Output: pin SWPORT						
$I_{sink(max)}$	maximum sink current	data byte CONTROL bit FLAG = 1; V_o = 0.4 V	1.0	-	-	mA

[1] Differential current on pins FREF1 and FREF2.

[2] The VCO frequency is determined by the external circuit at pins OSCFDB and OSCTNK.

[3] Conversion gain formula of DAA1: $V_{DAAOUT1} = \left(1.915 \times \frac{n}{128} + 0.1\right) \times V_{tune}$ where n = 0 to 127.

[4] Conversion gain formula of DAA2: $V_{DAAOUT2} = \left(0.693 \times \frac{n}{16} + 0.7\right) \times V_{DAAOUT1}$ where n = 0 to 15.

[5] The sink current must be limited to 18 mA by the external circuit.

[6] Input parameters of AM mixer measured between pins AMMIXIN and AMMIXDEC.

[7] Output parameters of AM mixer measured between pins AMMIXOUT1 and AMMIXOUT2.

[8] Input parameters of FM mixer measured between pins FMMIXIN1 and FMMIXIN2.

[9] Output parameters of FM mixer measured between pins FMMIXOUT1 and FMMIXOUT2.

[10] Input parameters of AM IF amplifier measured between pins AMIFAGCIN and IFAGCDEC.

[11] Output parameters of IF AGC amplifier measured between pins IFOUT1 and IFOUT2.

[12] Input parameters of FM IF amplifier measured between pins FMIFAGCIN1 and IFAGCDEC.

[13] Input parameters of FM IF amplifier measured between pins FMIFAGCIN2 and IFAGCDEC.

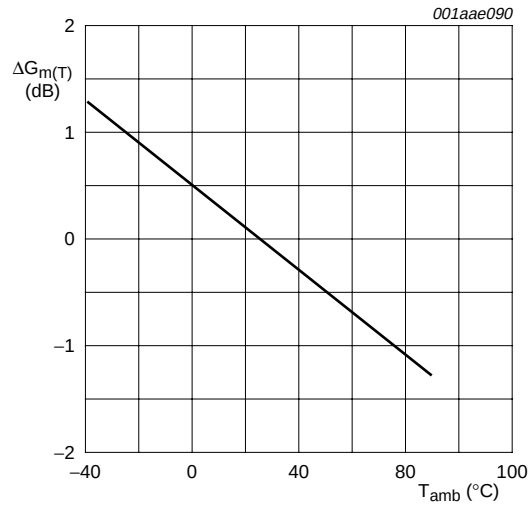


Fig 19. AM LNA transconductance gain deviation over temperature (including application)

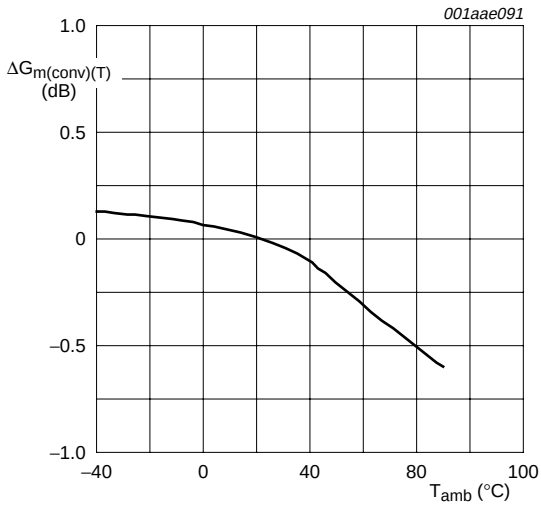


Fig 20. AM mixer conversion transconductance gain deviation over temperature (including application)

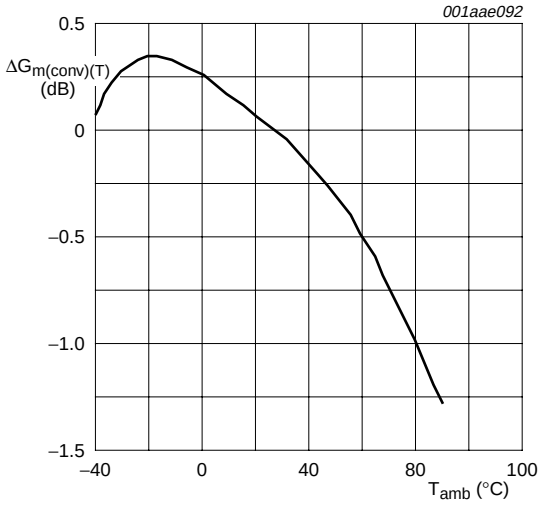


Fig 21. FM mixer conversion transconductance gain deviation over temperature (including application)

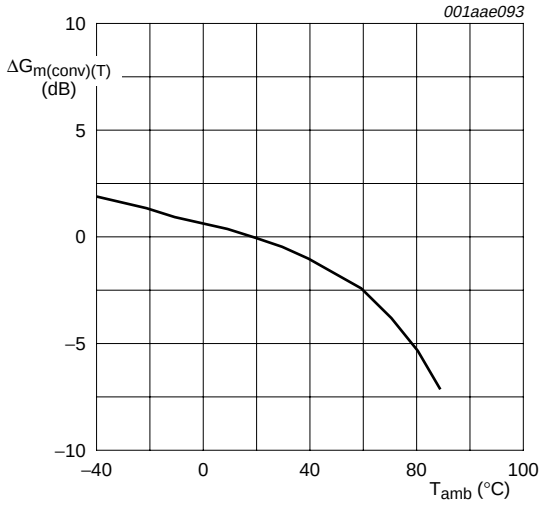


Fig 22. Weather band mixer conversion transconductance gain deviation over temperature (including application)

13. I²C-bus characteristics

The TEF6730AHW complies with the fast-mode I²C-bus protocol. The maximum I²C-bus communication speed is 400 kbit/s.

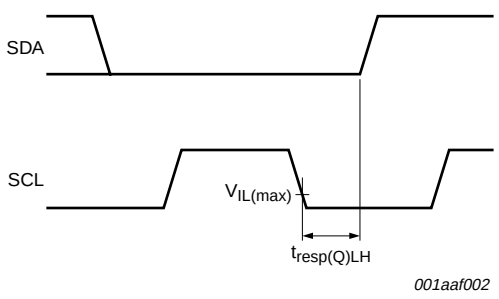
SDA and SCL HIGH and LOW internal thresholds are specified according to an I²C-bus voltage range from 2.5 V to 3.3 V including I²C-bus voltage tolerances of ±10 %. The I²C-bus interface tolerates also SDA and SCL signals from a 5 V bus. Restrictions for V_{IL} in a 5 V application can be derived from Table 37.

Table 37. I^2C-bus parameters

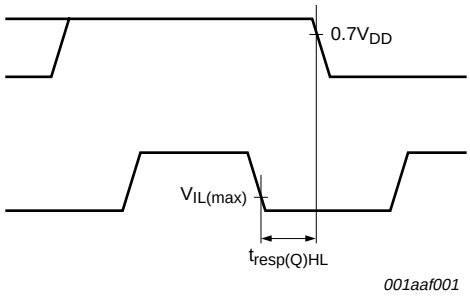
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage			-	-	1.09	V
V_{IH}	HIGH-level input voltage			1.56	-	-	V
C_i	capacitance for each I/O pin	pin SDA		-	4	6	pF
		pin SCL		-	3	5	pF
$t_{resp(Q)HL}$	HIGH-to-LOW data output response time	acknowledge and read data; see Figure 23					
		V_{DD} = 5 V; I = 3 mA; C_b = 400 pF		-	700	863	ns
		V_{DD} = 3.3 V; R_p = 1.8 kΩ; C_b = 400 pF		-	570	668	ns
		V_{DD} = 2.5 V; R_p = 35 kΩ; C_b = 10 pF		-	520	593	ns
$t_{resp(Q)LH}$	LOW-to-HIGH data output response time	read data; see Figure 23		-	450	488	ns
t_{of}	output fall time from V_{IHmin} to V_{ILmax}	C_b = 10 pF to 120 pF; see Figure 24	[1]	20 + 0.1C_b	10 × V_{DD}	-	ns
		$C_b \geq$ 120 pF; see Figure 24	[1][2]	20 + 0.1C_b	-	250	ns

[1] Minimum value of t_{of}; C_b = total capacitance of one I^2C-bus line [pF].

[2] Typical value of t_{of}; the output fall time t_{of} [ns] depends on the total load capacitance C_b [pF] and the I^2C-bus voltage V_{DD} [V]: $t_{of} = {}^{1}/_{12} \times V_{DD} \times C_b$.



a. Data change from LOW to HIGH



b. Data change from HIGH to LOW

Fig 23. Data output response time of the IC

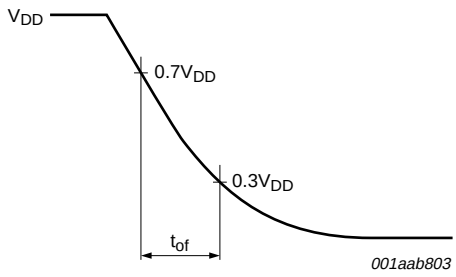


Fig 24. Definition of the fall time of the output signal

14. Overall system parameters

Table 38. Overall system parameters

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM overall system parameters[1]						
$f_{i(RF)}$	RF input frequency	LW	144	-	288	kHz
		MW	522	-	1710	kHz
		SW	2.3	-	26.1	MHz
f_{IF}	IF frequency		-	10.7	-	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB	-	50	-	µV
$V_{i(RF)}$	RF input voltage	start level of wideband AGC				
		data byte AGC bits WBAGC[1:0] = 00	-	125	-	mV
		data byte AGC bits WBAGC[1:0] = 01	-	100	-	mV
		data byte AGC bits WBAGC[1:0] = 10	-	75	-	mV
		data byte AGC bits WBAGC[1:0] = 11	-	35	-	mV
$V_{i(RF)M}$	peak RF input voltage	start level of narrow-band AGC; m = 0				
		data byte AGC bits NBAGC[1:0] = 00	-	200	-	mV
		data byte AGC bits NBAGC[1:0] = 01	-	170	-	mV
		data byte AGC bits NBAGC[1:0] = 10	-	140	-	mV
		data byte AGC bits NBAGC[1:0] = 11	-	115	-	mV
IP2	second-order intercept point	referenced to receiver input	-	152	-	dBµV
IP3	third-order intercept point	referenced to receiver input				
		Δf = 40 kHz	-	130	-	dBµV
		Δf = 100 kHz	-	133	-	dBµV
α_{ripple}	ripple rejection	$V_{CC(ripple)}$ / V_{audio}; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 10 mV (RMS); $V_{i(RF)}$ = 1 mV to 1 V	-	40	-	dB
FM overall system parameters[2]						
$f_{i(RF)}$	RF input frequency	FM standard	65	-	108	MHz
		weather band	162.4	-	162.55	MHz
f_{IF}	IF frequency		-	10.7	-	MHz

Table 38. Overall system parameters *…continued*

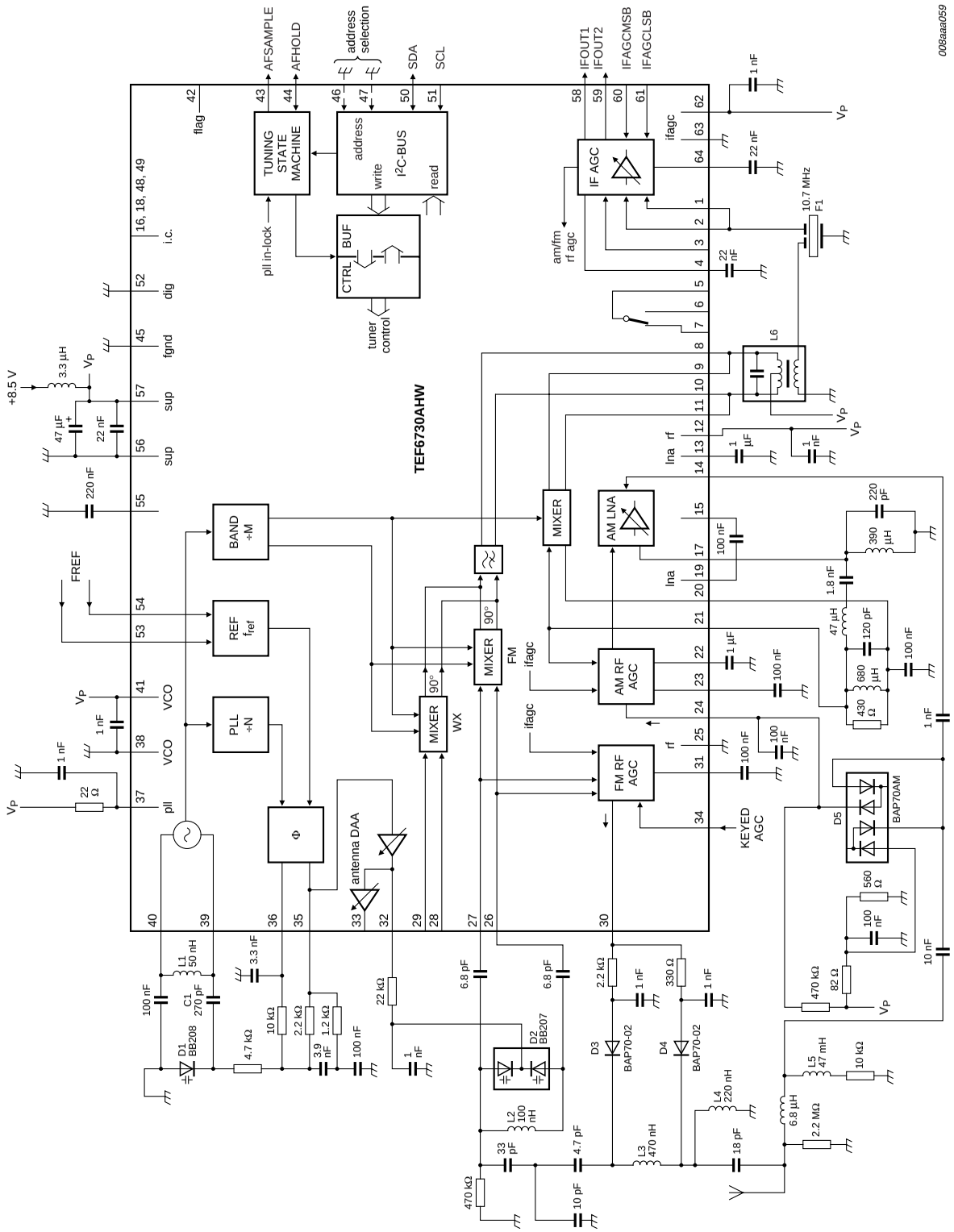
V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{sens}	sensitivity voltage	B_{IF} = 170 kHz	-	2	-	µV
		threshold extension enabled; weak signal handling enabled (SAF7730 N231)	-	1.1	-	µV
$V_{i(RF)}$	RF input voltage	start level of wideband AGC				
		data byte AGC bits WBAGC[1:0] = 00	-	19	-	mV
		data byte AGC bits WBAGC[1:0] = 01	-	14	-	mV
		data byte AGC bits WBAGC[1:0] = 10	-	10	-	mV
		data byte AGC bits WBAGC[1:0] = 11	-	7	-	mV
$V_{i(RF)M}$	peak RF input voltage	start level of narrow-band AGC; m = 0				
		data byte AGC bits NBAGC[1:0] = 00	-	17	-	mV
		data byte AGC bits NBAGC[1:0] = 01	-	14	-	mV
		data byte AGC bits NBAGC[1:0] = 10	-	11	-	mV
		data byte AGC bits NBAGC[1:0] = 11	-	9	-	mV
IP3	third-order intercept point	Δf = 400 kHz	-	123	-	dBµV
α_{ripple}	ripple rejection	$V_{CC(ripple)}$ / V_{audio}; f_{ripple} = 100 Hz; $V_{CC(ripple)}$ = 10 mV (RMS); $V_{i(RF)}$ = 500 µV	-	64	-	dB

[1] Based on 15 pF/60 pF dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, 2.5 kHz audio bandwidth, $f_{i(RF)}$ = 990 kHz, m = 0.3 and nominal maximum IF AGC gain, unless otherwise specified.

[2] Based on 75 Ω dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, de-emphasis = 50 µs, $f_{i(RF)}$ = 97.1 MHz, Δf = 22.5 kHz, nominal mixer gain and nominal maximum IF AGC gain, unless otherwise specified.

15. Application information



For list of components see Table 39.

Fig 25. Application diagram of TEF6730AHW

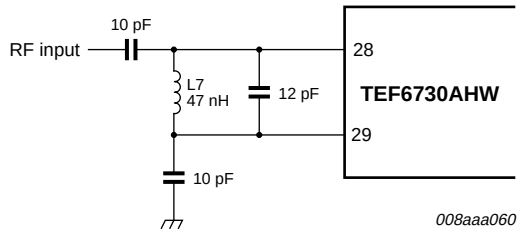


Fig 26. Weather band application

Table 39. List of components for Figure 25 and Figure 26

Symbol	Component	Type	Manufacturer
C1	capacitor for VCO tuning	270 pF; type NP0	-
L1	VCO coil	50 nH; E558CNA-100035	TOKO
L2	FM input coil	100 nH; C2520C-R10	SAGAMI
L3	FM antenna coil	470 nH; C2520C-R47	SAGAMI
L4	FM antenna coil	220 nH; C2520C-R22	SAGAMI
L5	AM mains suppression coil	47 mH; 388BN-1211Z	TOKO
L6	10.7 MHz IF coil	PF670CCS-A065DX	TOKO
L7	weather band input coil	47 nH; LQW31H	muRata
D1	VCO variable capacitance diode	BB208	NXP Semiconductors
D2	FM RF selectivity variable capacitance diode	BB207	NXP Semiconductors
D3	FM PIN diode	BAP70-02	NXP Semiconductors
D4	FM PIN diode	BAP70-02	NXP Semiconductors
D5	AM PIN diode	BAP70AM	NXP Semiconductors
F1	10.7 MHz IF ceramic filter	SFELA10M7HAA0-B0	muRata

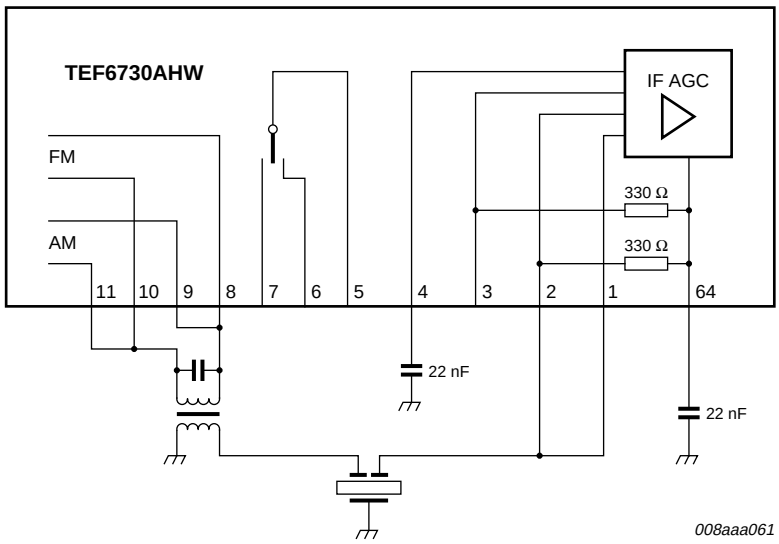


Fig 27. FM and AM mode

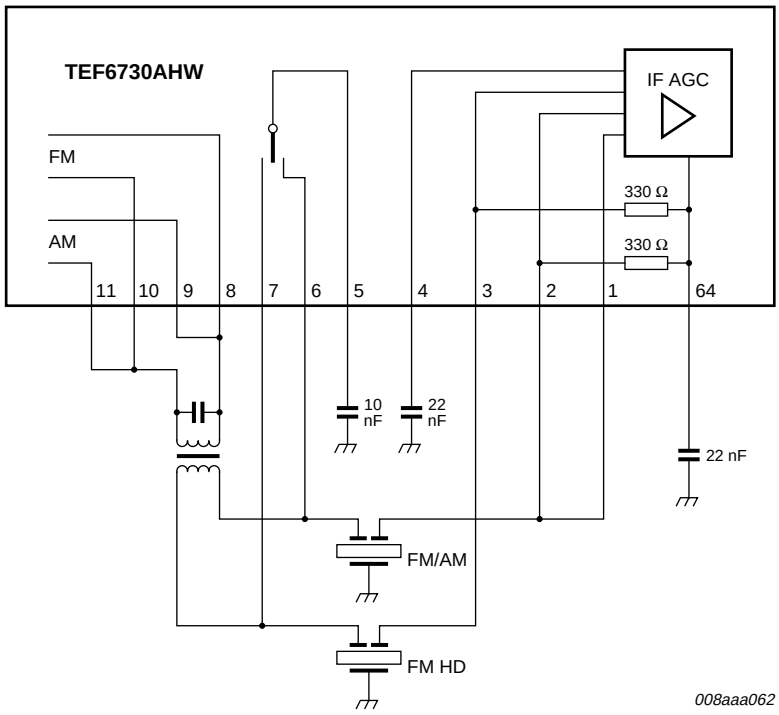


Fig 28. FM/AM and FM HD mode

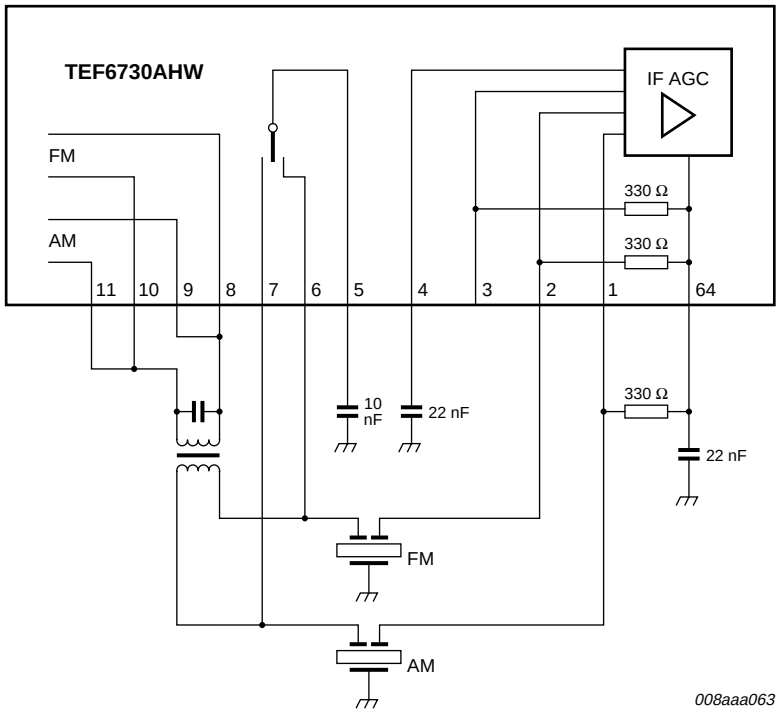


Fig 29. FM and AM (narrow band) mode

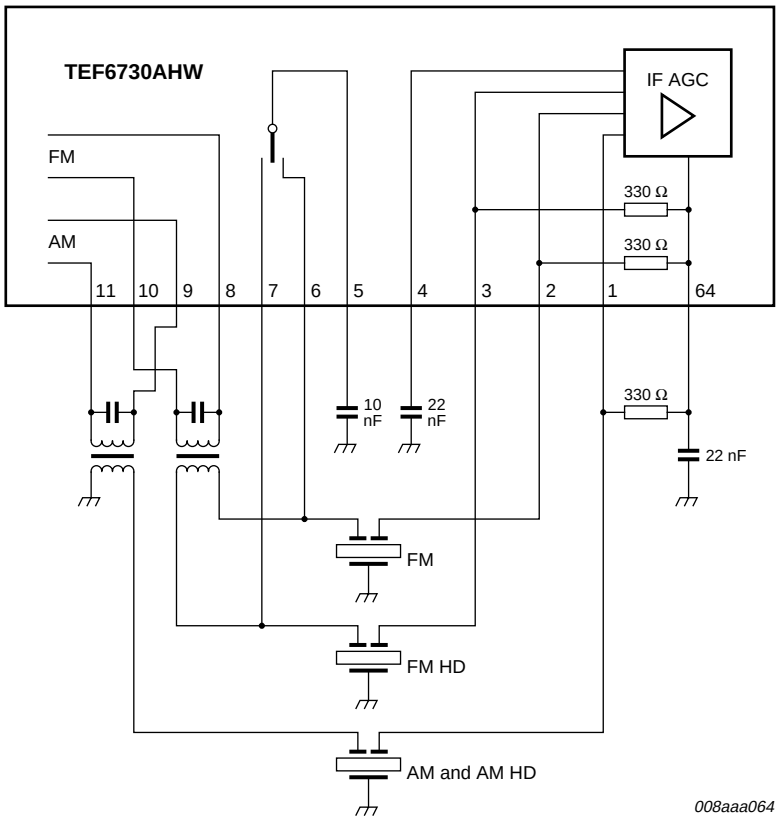


Fig 30. FM, AM, AM HD and FM HD mode

16. Test information

Table 40. DC operating points

Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
AMIFAGCIN	1	-	2.3	-	-	2.3	-
FMIFAGCIN1	2	-	2.3	-	-	2.3	-
FMIFAGCIN2	3	-	2.3	-	-	2.3	-
IFAGCDEC	4	-	2.3	-	-	2.3	-
SWDEC	5	-	1.4	-	-	1.4	-
CFSW1	6	-	1.4	-	-	1.4	-
CFSW2	7	-	1.4	-	-	1.4	-
FMMIXOUT1	8	external 8.5			external 8.5		
AMMIXOUT2	9	external 8.5			external 8.5		
FMMIXOUT2	10	external 8.5			external 8.5		
AMMIXOUT1	11	external 8.5			external 8.5		
$V_{CC(RF)}$	12	external 8.5			external 8.5		
V50LNA	13	-	5.2	-	-	0.9	-

Table 40. DC operating points *…continued*

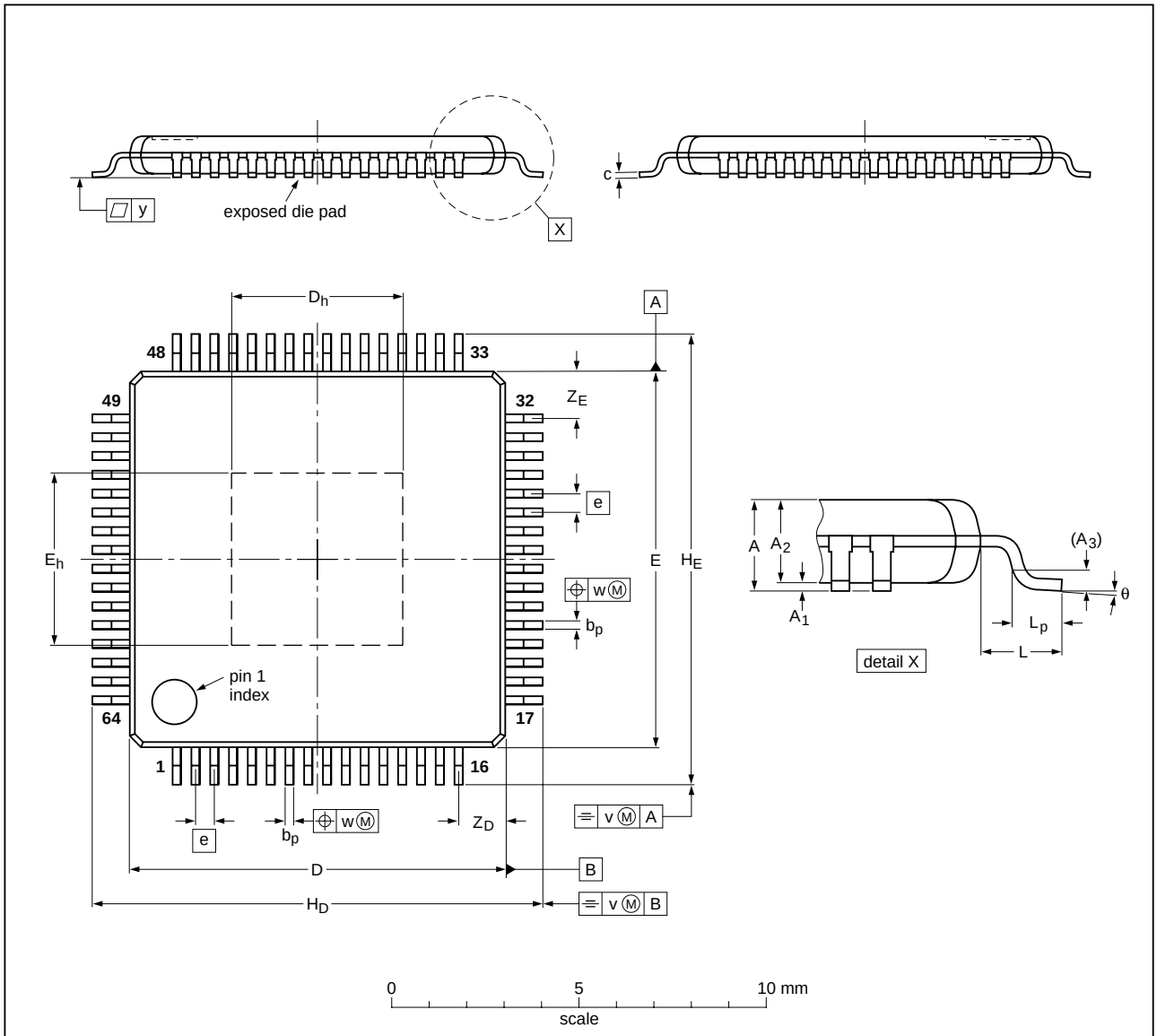
Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
LNAIN	14	-	1.9	-	-	0.1	-
AGCCNTRL	15	-	4.7	-	-	0.9	-
i.c.	16	-	-	-	-	-	-
LNAOUT	17	-	0	-	-	0	-
i.c.	18	-	-	-	-	-	-
LNAAGCDEC	19	-	5.2	-	-	0.8	-
AMMIXDEC	20	-	3.9	-	floating		
AMMIXIN	21	-	3.9	-	floating		
TAMAGC	22	-	1.4	-	floating		
PINAGCDEC	23	-	1.1	-	-	1.1	-
IAMAGC	24	external biasing			external biasing		
RFGND	25	external GND			external GND		
FMMIXIN1	26	-	0	-	FM: 2.4; WB: 0	FM: 2.8; WB: 0	FM: 3.2; WB: 0
FMMIXIN2	27	-	0	-	FM: 2.4; WB: 0	FM: 2.8; WB: 0	FM: 3.2; WB: 0
WXMIXIN	28	-	0	-	WB: 2.0; FM: 0	WB: 2.4; FM: 0	WB: 2.8; FM: 0
WXMIXDEC	29	-	0	-	WB: 2.0; FM: 0	WB: 2.4; FM: 0	WB: 2.8; FM: 0
IFMAGC	30	-	0	-	external biasing		
TFMAGC	31	-	0.8	-	-	0.8	-
DAAOUT1	32	0.5	-	$V_{CC(PLL)} - 0.6$	0.5	-	$V_{CC(PLL)} - 0.6$
DAAOUT2	33	0.5	-	$V_{CC(PLL)} - 0.7$	0.5	-	$V_{CC(PLL)} - 0.7$
KAGC	34	-	6.6	-	-	6.5	-
VTUNE	35	0	-	8.5	0	-	8.5
CPOUT	36	0	-	8.5	0	-	8.5
$V_{CC(PLL)}$	37	external 8.5			external 8.5		
VCOGND	38	external GND			external GND		
OSCFDB	39	-	5.8	-	-	5.8	-
OSCTNK	40	-	5.8	-	-	5.8	-
$V_{CC(VCO)}$	41	external 8.5			external 8.5		
SWPORT	42	external			external		
AFSAMPLE	43	-	0	-	-	0	-
AFHOLD	44	-	5	-	-	5	-
FGND	45	external GND			external GND		
ADDR2	46	external 8.5 or external GND			external 8.5 or external GND		
ADDR1	47	external 8.5 or external GND			external 8.5 or external GND		
i.c.	48	-	-	-	-	-	-
i.c.	49	-	-	-	-	-	-
SDA	50	external I^2C-bus voltage			external I^2C-bus voltage		
SCL	51	external I^2C-bus voltage			external I^2C-bus voltage		
DGND	52	external GND			external GND		

Table 40. DC operating points *…continued*

Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
FREF1	53	-	1.2	-	-	1.2	-
FREF2	54	-	1.2	-	-	1.2	-
VREF	55	4.1	4.3	4.5	4.1	4.3	4.5
GND	56	external GND			external GND		
V_{CC}	57	external 8.5			external 8.5		
IFOUT1	58	-	5.5	-	-	5.5	-
IFOUT2	59	-	5.5	-	-	5.5	-
IFAGCMSB	60	external 0 or external 3.3			external 0 or external 3.3		
IFAGCLSB	61	external 0 or external 3.3			external 0 or external 3.3		
$V_{CC(IF)}$	62	external 8.5			external 8.5		
IFGND	63	external GND			external GND		
IFAGCBIAS	64	-	2.3	-	-	2.3	-

17. Package outline

HTQFP64: plastic thermal enhanced thin quad flat package; 64 leads; body 10 x 10 x 1 mm; exposed die pad **SOT855-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.12 0.05	1.05 0.95	0.25	0.27 0.17	0.18 0.12	10.1 9.9	4.7 4.5	10.1 9.9	4.7 4.5	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT855-1		MS-026				~~04-05-18~~ 05-05-11

Fig 31. Package outline SOT855-1 (HTQFP64)

18. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 41 and 42

Table 41. SnPb eutectic process (from J-STD-020C)

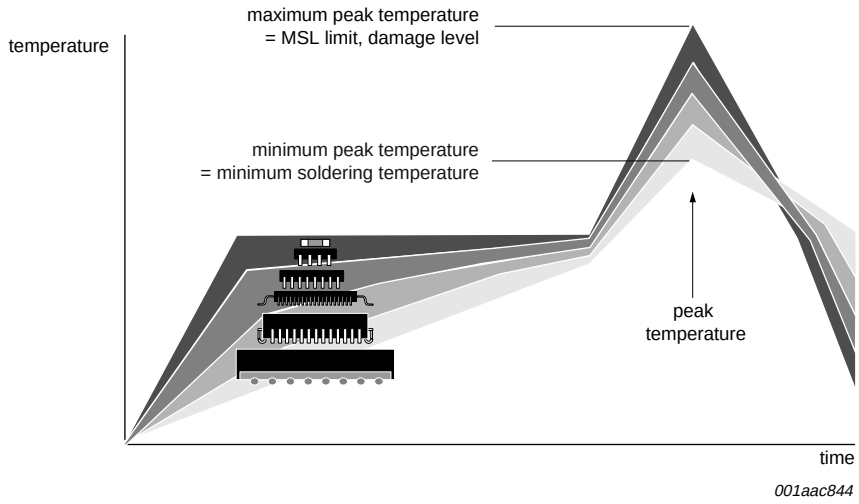
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 42. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



MSL: Moisture Sensitivity Level

Fig 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Footprint for soldering

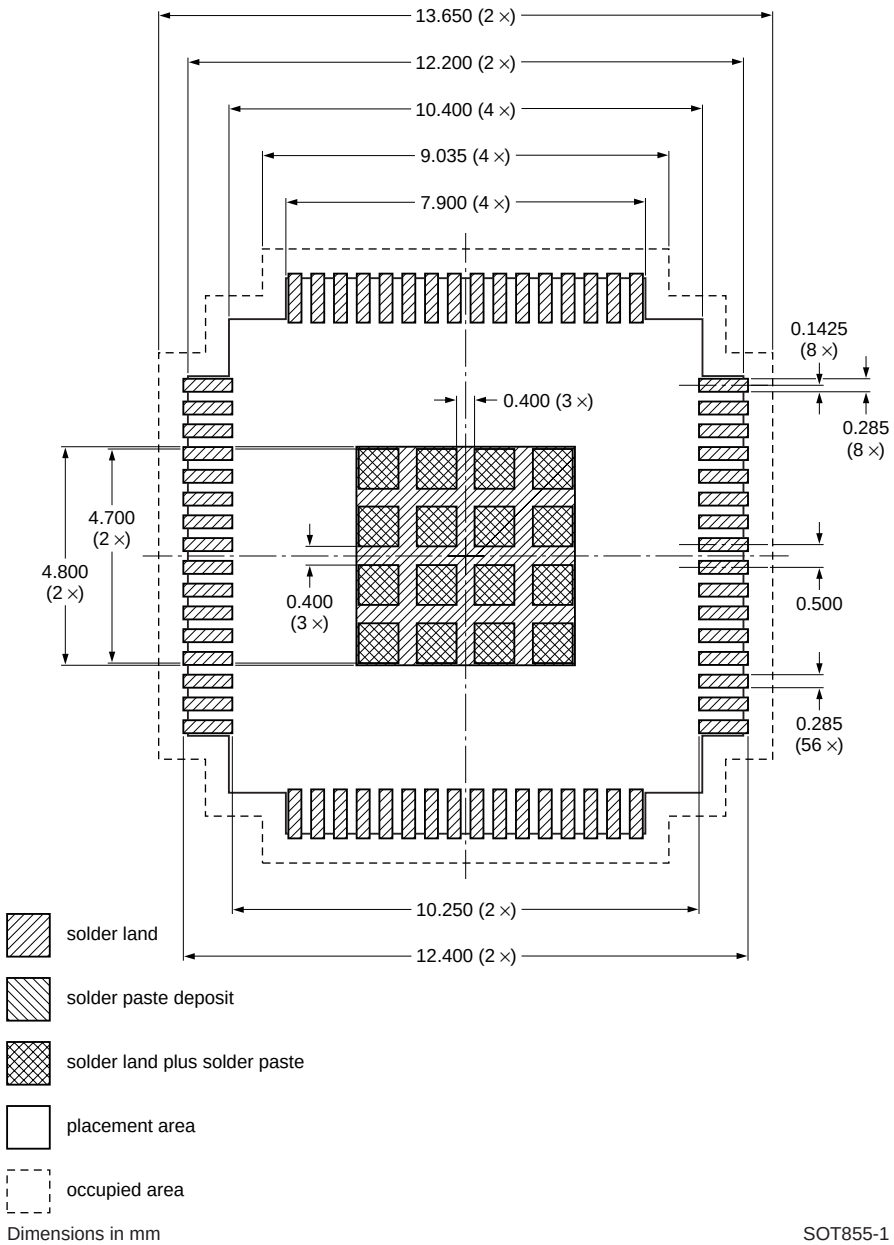


Fig 33. Footprint

20. Abbreviations

Table 43. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AF	Alternative Frequency
AFU	Alternative Frequency Updating
AGC	Automatic Gain Control
DAA	Digital Auto Alignment
DSP	Digital Signal Processor
DX	Distance
HD	High Definition
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
LW	Long Wave
MSB	Most Significant Bit
MW	Medium Wave
PIN	Positive Intrinsic Negative
PLL	Phase-Locked Loop
RF	Radio Frequency
SCL	Serial Clock
SDA	Serial Data
SW	Short Wave
VCO	Voltage-Controlled Oscillator
WB	Weather Band

21. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEF6730A_1	20070221	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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23. Contact information

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